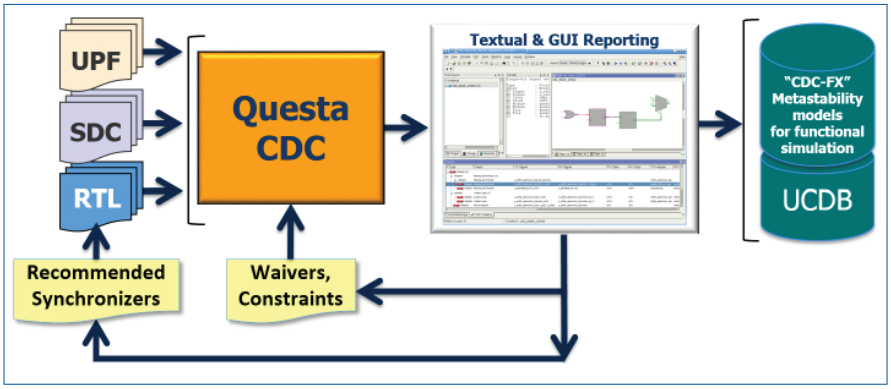
Questa Clock-Domain Crossing



Using only your RTL (and SDC constraints or UPF power intent files), Questa® CDC solutions automatically generate and analyze assertions to guard against chip-killing clock-domain crossing (CDC) issues. Metastability models can be exported to Questa Simulation for further analysis, and all results can be transmitted to the master verification progress database via UCDB. No knowledge of formal or property specification languages is required.

The High Risk of Multiple Clock Domains

Designers increasingly use advanced multi-clock architectures to meet the high-performance and low-power requirements of their chips. An RTL or gate-level simulation of a design that has more than one clock domain does not accurately model the silicon behavior related to the transfer of data between asynchronous clock domains. As a consequence, simulation does not accurately predict silicon functionality, risking show-stopper bug escapes.

Automated, Exhaustive, Easy-to-Use CDC Verification

Questa® CDC identifies errors using structural analysis to recognize clock domains, synchronizers, and low power structures via the Unified Power Format (UPF). It generates assertions for protocol verification along with metastability models for reconvergence verification. All properties and design intent are inferred by the software.

The technology exhaustively checks all potential CDC failures, statically verifying that all signals crossing asynchronous clock domain boundaries are guarded by CDC synchronizers. It then illustrates DUT issues found with familiar schematic and waveform displays. Additionally, in concert with Questa simulation, the CDC-FX app injects metastability into RTL functional simulation to verify the DUT is tolerant of random delays caused by metastability.

Industry-Leading Scalability and Quality of Results

When analyzing billion gate designs, minimizing "noise" is critical; i.e., how many issues does the CDC analysis detect, and are these issues real or false positives. Questa CDC's comprehensive, hierarchical, formal-based analysis searches through DUT elements for high throughput and noise minimization, simultaneously providing industry-leading scalability and high quality of results, while enabling CDC IP reuse.

FEATURES:

Automated solutions that target CDC verification challenges

- Structural verification
- Protocol verification (including assertions for both simulation & formal)
- Reconvergence verification

Easy set up

- Automated SDC import and debug
- Liberty model support
- Directly import Questa Simulation compiled libraries
- Xilinx and Altera FPGA library support

Easy to use for novices and experts

- Automatically infers clock grouping
- Automatically identifies CDC synchronization structures
- Recognizes over 50 synchronization styles
- Supports custom synchronizers for proprietary synchronization styles

Progress metrics at every step

- Structural report on all CDC paths and clock and reset trees
- Coverage for all CDC protocol assertions
- Coverage for all CDC-FX metastability models for simulation

Easy results analysis and debug

- Waiver management flow enables violation & waiver tracking throughout the design process
- Powerful Tcl API for funneling CDC data into custom reports
- Questa Verification Manager integration automatically generates test plans and trend reports

Power Aware CDC verification support

- Supports UPF 2.0 and 2.1
- Considers all isolation and retention cells
- Analyzes power domains with dynamic voltage and frequency scaling (DVFS)
- Verifies voltage domain crossings (VDC)

Benefits and Highlights

Immediate Productivity — Questa CDC automatically identifies your clocks and clock distribution strategy, minimizing set up time. Simply read in your RTL design and Questa CDC will pinpoint all potential CDC issues and recommend how to resolve them – no testbench is required.

Automated Repair Guidance — Questa CDC automatically identifies CDC synchronization structures, choosing from over 50 included synchronization styles. Users can also create and include custom synchronizers for proprietary synchronization styles.

Ease of Set Up and Use — Questa CDC supports the Synthesis Design Constraints (SDC) format for clock and port domain settings, and it includes a TCL scripting environment with powerful control and reporting capabilities. Clock groupings are automatically inferred and reported.

Low Noise, High Accuracy — Questa CDC produces the fewest false negatives in the industry, so users do not waste time chasing non-issues.

Low Power Intent Awareness — Questa CDC accepts your UPF file without modification to ensure low power circuitry does not introduce CDC-related issues. Specifically, Questa CDC considers all isolation and retention cells, power domains with dynamic voltage and frequency scaling (DVFS), and verifies voltage domain crossing (VDC) paths.

Familiar Visualization — CDC-centric analysis and debugging GUI leverages familiar, color-coded schematics and waveforms, linked to your HDL and UPF.

SoC-Level Scalability — Questa CDC's high performance analysis can process billion-gate designs, and its hierarchical approach enables unlimited capacity.

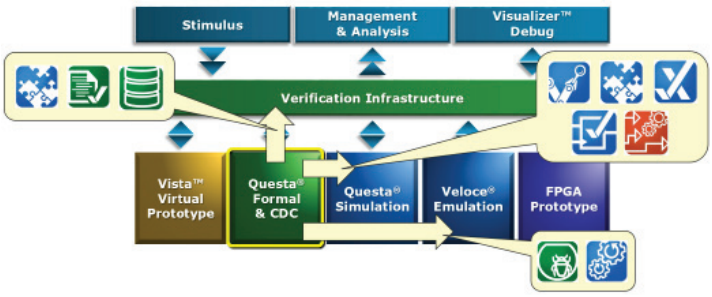
High Performance Analysis — Dedicated applied research and engineering investment in Questa CDC technologies have produced continuous improvements in wall clock performance, memory usage, and storage consumption. This means Questa CDC regularly exceeds demanding scalability and compute resource expectations.

Direct Integration with Questa Simulation — Patented, automated metastability injection is the only way to find complex CDC reconvergence bugs.

Verification Management — Automatic test plan generation and coverage reporting for static CDC analysis, protocol analysis, and reconvergence verification (via UCDB) enables you to measure CDC verification progress and the quality of the testbench with respect to CDC protocols, effectively managing the overall verification process.

Part of the Enterprise Verification Platform

Built upon several powerful technologies and tightly integrated with Veloce® emulation, the Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources. The Questa CDC and Formal solutions are integrated with simulation and emulation, sharing common features such as verification management, compilers, debuggers, and language support for SystemVerilog, Verilog, VHDL, UPF, and more. This enables users to select the best application or tool for the job, and then combine results from all the engines to dynamically track the progress of the entire verification program.



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