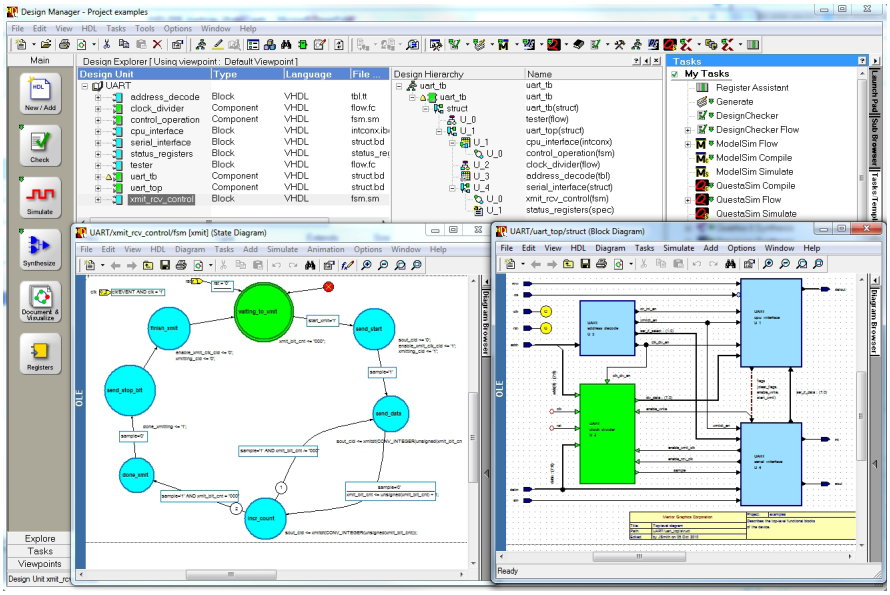
FPGA Design Creation

HDL Designer

D A T A S H E E T



HDL Designer is a powerful HDL-based environment used by individual engineers and engineering teams worldwide to analyze, create and manage complex FPGA and ASIC designs.

FEATURES AND BENEFITS:

- Ensures a structured FPGA/ASIC design flow
- Delivers a flexible environment for upstream and downstream tools and processes
- Reduces design creation time through automation and also code and diagram generation
- Supports consistent RTL coding through flexible design checking
- Assures SW- and HW-addressable register consistency
- Greatly aids design reuse
- Enables rapid and easy documentation with visualization and HTML snapshots
- Helps meet safety standards compliance mandates

Overview

HDL Designer is a powerful HDL-based environment which delivers new approaches to design today's most complex FPGAs and ASICs. HDL Designer is used worldwide by individual engineers and engineering teams to create, analyze and manage the design of these amazing devices.

HDL Designer accelerates the productivity and predictability of the project by automating many flows and tasks. Automated rule checking, register generation and documentation and the powerful text, tabular and graphical creation editors save incredible amounts of engineering time and can minimize manually introduced errors. Tool integration and version management of the entire project help keep the team, tools and design process structured, but is still flexible enough through an API to augment existing design flows. Through this automation and project management, the overall quality of the project and resulting chip is improved and project risk greatly reduced.

By using HDL Designer, savings and cost avoidance can be recognized immediately through this automation and will continue with future projects through better design reuse, consistency of coding and improved documentation. For safety- and mission-critical projects, HDL Designer's design checking, version management, register generation and documentation support adherence to regulatory compliance mandates such as DO-254 and ISO 26262.

Project Management and Team-based Design

HDL Designer tackles the design management problem by automating and simplifying project and team management throughout the design flow. HDL Designer provides the designer and design team with interfaces to other design tools within the flow including ReqTracer, Questa/ModelSim, Precision, and FPGA vendor and other EDA tools for automated compilation, simulation, invoke and interactive debug. To ensure consistency, teams use the same preferences, tools, tool versions, coding templates and tasks to automate repetitive flows. The flexible project import and API enable HDL Designer to easily fit into existing design processes and to build custom design flows.

The simplified version management systems interface manages all design project related data for an individual or team of engineers. HDL Designer supports Subversion, IBM® ClearCase, CVS, RCS, Dassault® DesignSync, CliosSoft SoS™ and Microsoft® VSS.

Documentation of the complete project is easily created via OLE, print and graphics export. Project snapshots in HTML reduce design review preparation time and documentation creation effort.

Automated Design Rule Checking

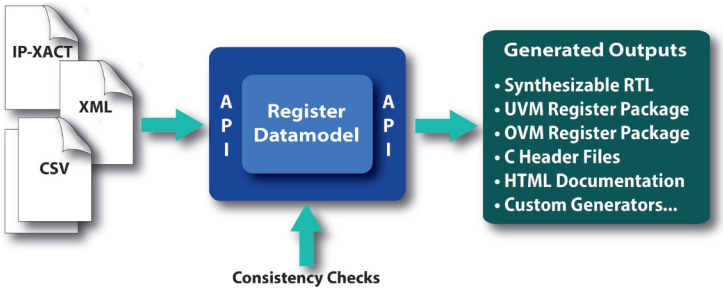
Automated design checking reduces project costs and improves the quality of the HDL code. The automation decreases the manual code review effort, speeds the HDL code checking, and identifies design flaws early in the development cycle—before simulation, synthesis and production—where it is less expensive and easier to correct the violations.

Design checking, which can be run interactively or via batched processes, identifies circuit implementation violations through the built-in synthesis engine, applies the checks design-wide to identify violations across module boundary crossings, and enforces coding style rules for readability, reusability and coding consistency. The seven pre-configured rulesets, including the DO-254 ruleset, assist in adopting design checking while parameterizable checks enable the creation of customized rulesets and policies.

Quality metrics and violations results are summarized in the design checking reports and speed the design review process. Violations are cross-referenced to the HDL code and graphical source views to aid debug.

Register Automation

The Register Assistant feature generates software- and hardware-addressable registers and memory mappings in the formats required for all the engineers on the project, including the UVM/OVM Register Package for verification engineers, Synthesizable RTL for hardware designers, C header files for software developers and HTML documentation for documentation/information engineers.



Register Assistant accepts input from many sources and automates the generation of the required register formats.

By automating the creation of the registers for multiple supported formats, consistency of register information is guaranteed, hand coding and hand editing errors are eliminated, and a large amount of time is saved.

Improving Design Creation and Reuse

"Do I have all the required files?" "How well is this code written?" "How can I quickly understand what the code does?" HDL Designer answers all of these questions by providing HDL code integrity analysis, code quality assessment and code visualization for increased design comprehension to speed the incorporation of reused HDL code into the current project. For creation of new HDL code, HDL Designer offers intelligent text, graphical and tabular editors and the ModuleWare parameterized generator library.

Assisting in Design Assurance Compliance

Design assurance and safety-critical designs are required to adhere to specified design processes to ensure that the FPGA or ASIC meets the required safety standards for such design areas as commercial aircraft, automotive electronics and medical equipment and devices. HDL Designer's version management, register automation and design checking capabilities can assist in meeting these design assurance mandates.

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

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