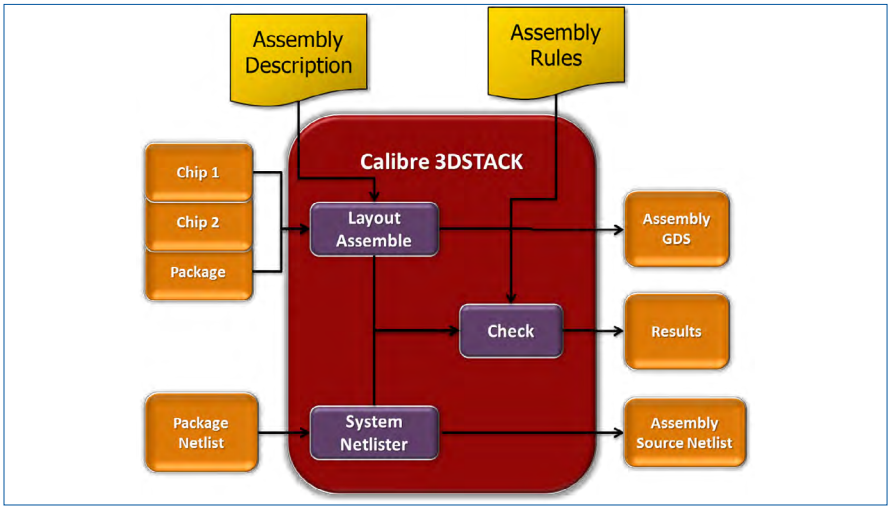
3D-IC Verification
Calibre® 3DSTACK

Physical Verification

D A T A S H E E T



Calibre 3DSTACK enables signoff verification of chip stacks with flip chips, silicon interposers, through-silicon vias, and more.

3D-IC Stack Verification

While standard Calibre product offerings support foundry-qualified design rule checking (DRC) and layout vs. schematic (LVS) comparison of individual dies, Calibre 3DSTACK extends Calibre die-level signoff verification to enable complete design verification of stacked die assemblies. Calibre 3DSTACK can be used for verification of a wide variety of stacked die assemblies, such as stacked memories, stacked sensor arrays, interposer-based structures, or package-level routing (wafer-level packaging).

Calibre 3DSTACK enables assembly-level verification of the packaging interfaces. It operates on the interface geometries between chip designs, including bumps, balls, through-silicon vias (TSVs), or copper-to-copper bonding, and can support dies from multiple processes with ease. Based on package information in a rule deck (die order, x/y position, rotation and orientation, etc.), Calibre 3DSTACK performs all DRC and LVS checking of complete multi-die 2.5D-IC and 3D-IC systems. Calibre 3DSTACK is enabled using standard Calibre DRC, Calibre LVS and Calibre DESIGNrev license features—no new licenses are required. What's more, Calibre 3DSTACK delivers these capabilities without breaking current tool flows or requiring new data formats.

Why Calibre 3DSTACK?

Traditional DRC and LVS verification tools assume layers are co-planar, and that polygons located on the same GDSII layer are physically located on the same vertical plane. 2.5D and 3D structures contain multiple die that potentially contain polygons on the same GDSII layer, but at different vertical depths, and quite possibly representing completely different geometries. When 2.5D and 3D designs are verified with traditional tools, layer conflicts can appear to exist between multiple dies with the same layers.

FEATURES:

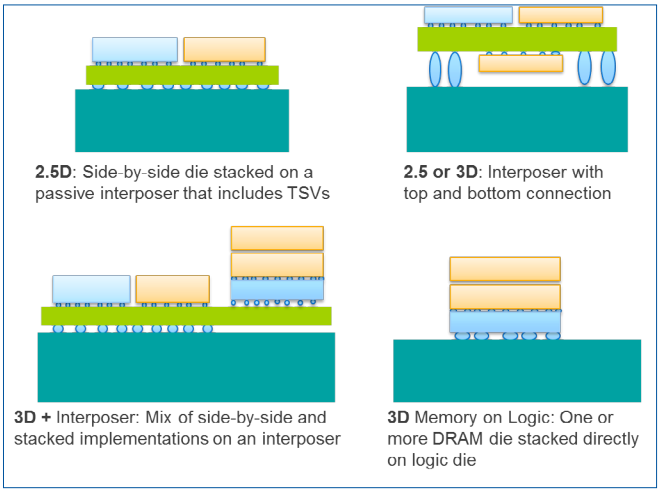
- Supports all types of stacked designs, including interposers, stacked memory, front-to-back TSV configurations, package-level routing, and more
- Supports multi-process configurations without the need for foundry-specific process rule files
- Enables connectivity tracing of passive interposers to identify shorts or opens
- Provides system netlist generator tool for creation of assembly source netlists or full assembly extracted netlists
- Extends existing Calibre licenses
- Included in TSMC CoWoS and InFO reference flows

BENEFITS:

- No new Calibre licenses or tools required
- Accurate DRC and LVS signoff verification of 2.5D and 3D assemblies
- Applicable to virtually any stacked design configuration
- Ensures signoff Calibre verification while reducing time-to-tapeout

Mentor Graphics®

Calibre 3DSTACK uniquely identifies geometries per layer per die placement in the assembly, allowing accurate checking between dies. By supporting flexible stacking configurations of multiple dies, Calibre 3DSTACK minimizes disruption to existing verification flows while providing designers with maximum flexibility across process nodes and stacking configurations (interposer-based and full 3D).



Typical 2.5D and 3D configurations that Calibre 3DSTACK can support.

With the ability to differentiate the layers of interest per individual die placement, Calibre 3DSTACK enables designers to verify the physical attributes (offset, scaling, rotation etc.) of each die, while also tracing the connectivity of the interposer or die-to-die interfaces.

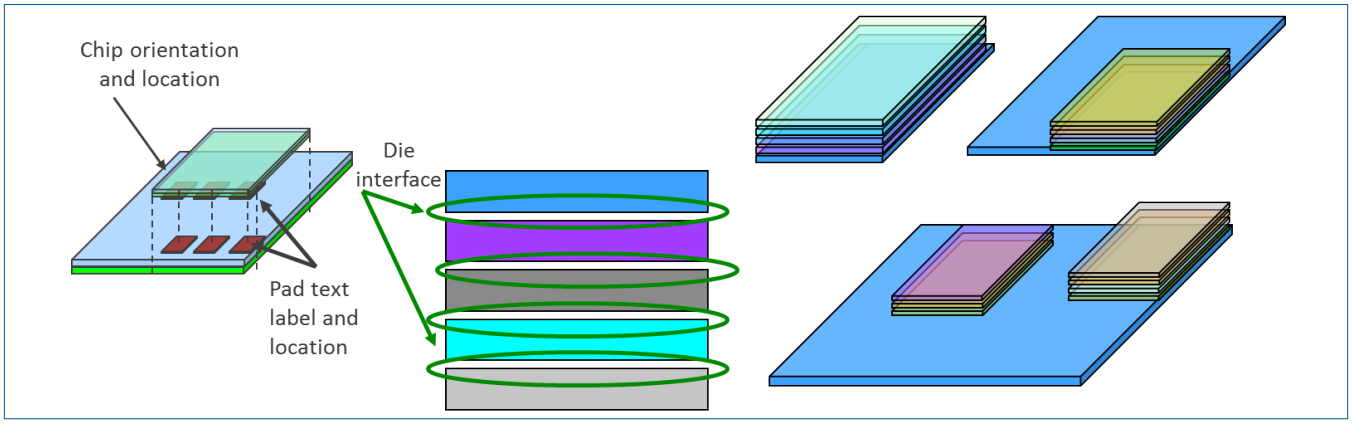
Calibre 3DSTACK obtains the required configuration information from the rule deck:

- List of dies in the assembly
- Information about each die's position (x/y, orientation, rotation)
- Text ports at the bump or pad locations
- Interface type, geometry, and materials

With this information, Calibre can perform all DRC and LVS checking of complete multi-die 2.5D-IC and 3D-IC systems. Calibre 3DSTACK also provides extendability, with the capacity to incorporate new extraction and verification solutions in the future.

Superior Product Support

Mentor Graphics is a five-time winner of the Software Technical Assistance Recognition (STAR) Award in EDA. No other provider of complex software can match the support offered by Mentor Graphics.



Calibre 3DSTACK uses information supplied in the rule deck to support the various stacking configurations.

For the latest product information, call us or visit: www.mentor.com

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