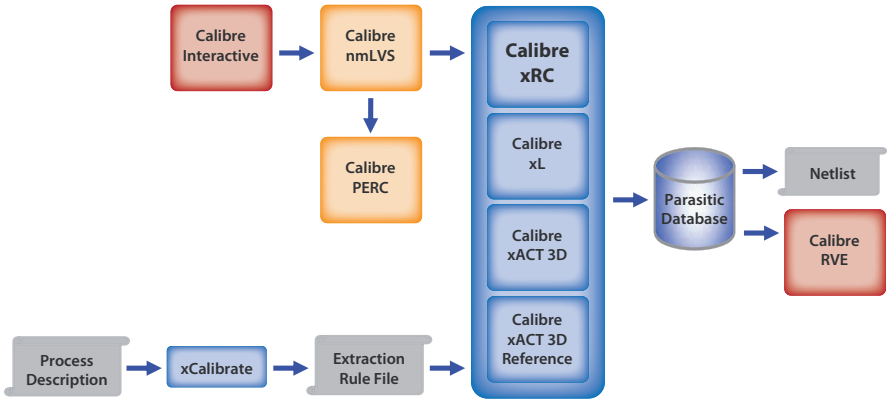
Fast, Accurate, Rule-Based Parasitic Extraction

Calibre xRC

Circuit Verification

D A T A S H E E T



Calibre xRC is fully integrated into the Calibre verification suite for seamless creation of netlists and parasitic debugging in the design environment using Calibre RVE. xCalibrate is used by foundries to create extraction rule files, and the same rule files can be used by Calibre xRC, Calibre xL, Calibre xACT 3D and Calibre xACT 3D Reference.

High-Performance Rule-Based Parasitic Extraction with Industry-Proven Accuracy

Calibre® xRC parasitic extraction gives designers rapid, accurate, and comprehensive feedback, increasing confidence that manufactured devices will function according to design. It seamlessly integrates with all major design flows because it is a constituent element of the industry-proven Calibre physical verification suite. With countless successful tapeouts to its name, foundry-qualified Calibre xRC signoff-quality rule decks in industry-standard SVRF format exist for practically every manufacturing process imaginable.

Hierarchical Extraction Reduces Simulation Time

Parasitic extraction tools can potentially generate a huge volume of data, impacting overall processing time including extraction and simulation of these very large netlists. The Calibre xRC product accelerates extraction and simulation in several ways:

- Leverages Calibre hierarchical design processing, greatly accelerating turnaround time particularly for designs that include regular arrays (e.g., memories), and multiple instances of hierarchical cells;
- Scales across multiple cores or CPUs using the Calibre multithreaded architecture;
- Accelerates time-to-simulation by providing sets of compact, transistor-level parasitic data that can be back-annotated and simulated while the extraction process is still running on other parts of the design;
- Combines mixed-level data (transistor-level, gate-level, and hierarchical), in a single parasitic extraction run;

BENEFITS:

- **Full-chip performance**—combines the performance of the Calibre hierarchical and multi-threaded architecture with a compact netlist to boost throughput of large designs and maintain rapid feedback within custom design environments. Multiple process corner analysis does not require complete design re-run.
- **Proven accuracy**—Advanced extraction and process models correlate closely with field solver results; proprietary reduction algorithm maintains integrity of parasitic data. Reduces need for prohibitive design margins by incorporating manufacturing-dependent effects (e.g., in-die variation) into parasitic models.
- **Rule deck availability**—Availability of foundry-certified signoff rule decks in SVRF format ensures Calibre xRC parasitic extraction can meet your design needs regardless of process or foundry choice.
- **Easy flow integration**—Calibre xRC exchanges native database information with Calibre nmLVS, Calibre PERC, and Calibre xACT 3D products. Upstream design integration using Calibre Interactive, CalibreView and Calibre RVE enables GUI-driven launch, back annotation, and cross-probing for all popular layout environments. Support for all major transistor-based and cell-based simulation and analysis netlist formats ensures compatibility with downstream digital, custom, and mixed-signal flows.

- Generates multiple netlists including any mixture of resistance, intrinsic capacitance, and coupling capacitance and based on multiple process corners without requiring a complete re-run;
- Generates compact netlists that accelerate simulation without sacrificing accuracy.

Engines Precisely Model Advanced Effects

The Calibre xRC capacitance engine's proven close correlation with field solver and silicon data provides the greatest contribution to the overall accuracy of the product. The engine incorporates precise, specific models for vias, contacts, and poly-to-contact area, which are particularly susceptible to esoteric but significant capacitance effects. Designers can control modeling around devices very accurately because of the product's close integration into Calibre LVS and Calibre xACT 3D.

The product's resistance engine delivers improved fracturing, including precise width and resistor location for electromigration analysis. It enables device pin handling and customized control over gate-region extraction. The engine's algorithms are hierarchical and correlate closely with resistance field-solver values.

Integration with Calibre Platform Ensures Efficient Data Handling

Calibre xRC parasitic extraction is fully integrated into the Calibre physical verification suite along with Calibre nmLVS (layout vs. schematic), and the Calibre xACT 3D field solver. This facilitates seamless data exchange and analysis using a combination of LVS, rule-based parasitic extraction, and field-solver–based parasitic extraction. This integration also helps the clear definition of the boundary between the device model and the parasitic tool, eliminating double counting of parasitics and ensuring that there are no missed effects.

Accelerates Mixed-Signal and Custom Design

Tight integration between the design environment, Calibre nmLVS, Calibre xRC parasitic extraction, and simulation and analysis tools streamlines data handling between upstream design creation environments and downstream post-layout analysis. The synergistic pairing of hierarchical Calibre nmLVS with Calibre xRC parasitic extraction gives analog/mixed-signal designers several performance and analysis benefits for full-chip, mixed-signal design:

- Enhanced accuracy for custom devices through intentional device recognition with exact device parameters;
- Ease of operation in a mixed-signal environment with concurrent transistor-level and gate-level parasitic device extraction;
- Acceleration of custom debug through seamless back-annotation of simulation results to the source schematic.

The optional Calibre results viewing environment (RVE) enables automated re-simulation directly from within the design layout environment. It allows designers to examine resistance, intrinsic capacitance, and coupling capacitance (R, C, RCC) data in a graphical environment, and it facilitates back-annotation and netlisting.

Designers who are using Calibre programmable electrical rule check (PERC) can drive electrostatic discharge analysis directly from Calibre xRC resistance data. Designers can search for specific topologies, identify pins and ports of interest, extract parasitic resistances between these pins and ports, and compare point-to-point resistance against constraints. Designers can then display violations using Calibre RVE.

Integrated with Multiple Design Flows

The product's flexible data model enables multiple diverse design flows and styles including analog, memory, ASIC, and mixed signal.

Calibre xRC parasitic extraction supports all popular upstream design tools because it directly reads hierarchical and flat layout data in standard formats including GDS, annotated GDS, LEF/DEF, and Milkyway.

The optional Calibre Interactive product enables interactive extraction driven from a graphical user interface (GUI), integrated into standard layout environments including Mentor Graphics Olympus SOC place-and-route, Mentor Graphics Pyxis custom layout and Calibre DESIGNrev, Cadence Virtuoso and Encounter, Synposys Milkway and IC Compiler, Seiko System SX9000, and SpringSoft Laker.

In digital flows, Calibre xRC establishes connectivity information directly from LEF/DEF or annotated GDS design data. This saves time and effort by eliminating the need for an additional LVS run. Calibre xRC enhances gate-level extraction accuracy because it supports a mixture of LEF/DEF and GDS information. This allows designers to incorporate GDS metal fill or transistor-level cell models without requiring a full GDS stream-out from place-and-route.

Calibre xRC operates seamlessly within multiple schematic and layout environments for easy debugging, and it generates standard netlist formats, including Hspice, Eldo, Spectre, Calibreview, DSPF, and SPEF. Calibre xRC drives fast, SPICE-level accurate, hierarchical, and flat circuit simulation and static-timing, signal-integrity, and IR-drop

analysis. Calibre xRC can optimize hierarchical netlist data for use with the Synopsys HSIM signal and power net analysis tool.

The parasitic reduction capability of Calibre xRC is based on a proprietary combination of AWE and S-parameter techniques with custom control of thresholds and tolerances.

The Calibre parasitic database provides customizable parasitic models per net (for example, R only, RCC, RCCLM), to enable different analysis flows, including noise, timing, power, and signal integrity.

Calibre Commitment to Innovation

Calibre leads the way for one powerful reason—our constant and ongoing commitment to innovation. We know that when you're ready to move to the next node, your tools need to be ready as well. You need the confidence that comes from knowing we've been working far in advance to identify the challenges and develop effective, proven solutions. Our reputation depends on it, and we depend on our reputation. At every node, Calibre has provided, and will continue to provide, pioneering technologies and tools that ensure you can continue to deliver your products on time with the quality you need.

The Calibre nm Platform

The Calibre nm platform, the industry's leading physical verification platform, is known for delivering best-in-class performance, accuracy, and reliability. A powerful hierarchical engine is at the heart of the Calibre tool suite, providing solutions for physical verification, parasitic extraction, resolution enhancement, mask data prep, litho-friendly design, and design for manufacturing.

Complete Calibre rule files and extensive coverage of Calibre processes for DRC and DFM are available at all major semiconductor foundries.

Superior Product Support

Mentor Graphics is a five-time winner of the Software Technical Assistance Recognition (STAR) Award in EDA. No other provider of complex software can match the support offered by Mentor Graphics.

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