08|2018

TRIAS TRAINING CENTER

ACCELERATING FPGA VHDL VERIFICATION

DESCRIPTION

A lot of time is wasted on inefficient design and lack of awareness and knowledge of the most critical digital design issues. Huge improvement potential can be realised just by making a few important changes to the way we design. The key is a well-structured testbench.

The course will concentrate on FPGA verification and how a well-structured testbench is constructed. Theory alternates with practical examples, as well as hands-on tutorials. It also covers important topics such as coverage, Bus Functional Models (BFM), debugging and randomization. This is also a great opportunity to get to know the Universal VHDL Verification Methodology (UVVM), which is freely accessible as open source, and can easily and quickly create a well-structured testbench.

After the course, participants will know how to structure an FPGA verification platform, how to implement their testbenches, and how to write test sequencers, which can be understood by software and hardware developers. Participants will also learn how to use the complete VHDL-based UVVM verification platform within their own organization

AGENDA

- Making a simple VHDL testbench step-by-step
- Using procedures and making good BFMs
- Applying logs, alerts, value and stability checkers, awaits, and more
- Making an advanced VHDL testbench step-by-step
- Assertions, randomization, constrained random, coverage, debuggers, monitors
- Verification components and testbench architecture for advanced verification
- Making testbenches as simple as possible – adapting to the DUT complexity
- Structuring, Debugging, Overview, Maintainability, Extendibility
- Examples and labs using UVVM

TARGET GROUP
FPGA and Digital ASIC Designer

PREREQUISITES
Knowledge of VHDL

DURATION
3 days

LANGUAGE
English

COURSE TARGETS
- Structure an FPGA-verification platform
- Improvement of your general working methodology
- Set up and use of UVVM framework
- Develop and use Bus Functional Models and VHDL Verification Components
- Reuse and modification of BFMs and VVCs with minimum effort
- Significant reduction of verification time

COSTS
€ 1.850,00 per participant*

www.trias-mikro.de

**including training materials, lunch and refreshments*

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TRIAS mikroelektronik GmbH

TRAINER

Espen Tallaksen

is the CTO and founder of Bitvis, an independent design centre for embedded software and FPGA.

He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway, including his earlier founded company Digitas. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement. One result of this interest is the UVVM verification platform that is currently being used by companies world-wide.

He has given many presentations and keynotes on various technical aspects of FPGA development including ABB Embedded Systems Forum, FPGAworld and at FPGA Kongress in Germany.

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FURTHER COURSES

- Accelerating FPGA and Digital ASIC Design

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