08|2018

TRIAS TRAINING CENTER

SYSTEMVERILOG
ADVANCED VERIFICATION FOR FPGA DESIGN

DESCRIPTION

Modern FPGA designs have tremendously advanced in both performance and capacity. Verification of this kind of designs has become a daunting task, especially the validation of the design against the specification and test plan.

SystemVerilog provides a comprehensive set of verification tools and is a natural extension to Verilog. It also provides constructs with clearer intent like enumerated types, integrated assertions and higher language constructs, which support design hierarchy and Object Oriented Programming (OOP). Powerful testbench features allow for more flexible and reusable testbench development, even in the context of a VHDL based design.

This workshop will give an overview about the SystemVerilog language and will introduce into new verification methodologies „Assertion Based Verification“, „Constrained Random Generation“ and „Functional Coverage“. The participant will learn how to use these powerful verification tools to speed up verification as well as to measure the verification progress and how these methodologies can be naturally applied to the verification of VHDL designs.

SHORT AGENDA

- Motivation
- Introduction to SystemVerilog
- SystemVerilog Assertions
- Constrained Randomization
- Functional Coverage

TARGET GROUP
FPGA design and verification engineers

PREREQUISITES
Experience with VHDL or Verilog for Design and Verification

DURATION
3 days

LANGUAGES
English or German

COURSE TARGETS
- Basic knowledge of SystemVerilog
- Basics of OOP in SystemVerilog
- Use of OOP for faster and more efficient, reusable testbench designs
- Knowledge of the concept of an automated testbench
- Introduction to assertions, constrained randomization and functional coverage

COSTS
€ 1.850,00 per participant*

www.trias-mikro.de

**Including training materials, lunch and refreshments*

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TRIAS mikroelektronik GmbH

TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikroelektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.

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ADDITIONAL COURSES

- UVM Made Easy for FPGA Designer
- VHDL 2008
- Verilog for VHDL User