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TRIAS TRAINING CENTER

UVM MADE EASY FOR FPGA DESIGNER

DESCRIPTION

Today's FPGA designs have become complex SoC type of designs which has driven the complexity to a level that used to be specific to ASICs some years in the past. For a complete verification of those systems, writing testbenches has become a challenging task. Different verification methodologies have addressed this on different levels. The most comprehensive approach is the Universal Verification Methodology, UVM. It has become a standard (IEEE 1800.2-2017). It provides SystemVerilog Verification base components that can be used to create a testbench infrastructure with a high reuse potential.

Since the UVM library is very complex building a testbench from scratch is a time-consuming task and requires a good knowledge of the tools the library provides. In order to help verification engineers to build a testbench infrastructure very quickly UVM Framework has been developed. With UVM Framework a UVM testbench can be created very rapidly and with a few changes the testbench is ready for simulation within a few hours.

The workshop UVM MADE EASY FOR FPGA DESIGNER will introduce to the most important UVM building blocks to provide a basic understanding how a UVM testbench looks like, how the component instance creation process works and how the verification components communicate with each other and the DUT.

AGENDA

- Introduction
- UVM
- UVM Verification Components
- UVM Transaction Interfaces
- UVM Factory
- UVM configuration database
- UVM Framework (UVMF)
- UVMF Base Classes
- UVMF Base Class Package
- Introducing the UVMF API

TARGET GROUP

FPGA design or verification engineers

PREREQUISITES

Knowledge of SystemVerilog and OOP concepts

DURATION

2 days

LANGUAGES

English or German

COURSE TARGETS

- Create a UVM testbench with the UVM Framework
- In multiple steps to a simple example DUT
- Guidance to the process to run a testcase
- Ability to use the UVM Framework API for testbench for own FPGA design

COSTS

€ 1.450,00 per participant*

www.trias-mikro.de

**Including training materials, lunch and refreshments*

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TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikroelektronik GmbH since 2002 and, as the technical manager, covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.

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ADDITIONAL COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- Verilog for VHDL User