… For complex processes, the DDR memory is used to temporary store data, to perform in time mathematics and to share data among various locations. High frequency clocks, data and other DDR signals are using hundreds MHz to several GHz in speed. As the frequency values increase, the high-speed issues (timing, integrity, noise) become disturbing factors for the equipment behavior. That is why signal integrity characterization is mandatory. It can be done on prototypes that are completely assembled but it would take a long time to validate the correct functionality, a cost on the prototypes and maybe the lack of experience on testing …

… The simulation environment **HyperLynx** developed by the company **Mentor Graphics** has implemented simulation capabilities that addresses any type of signal integrity issues. In terms of the DDRAMs, a wizard assists the user through the setup and simulation process. This is an option available at the BoardSim (pre-layout) level. The wizard includes enough know how to provide support even to the newbies in DDR technology. This kind of assistants are very useful for the designing process entitling the use with power in simulations that the pen and the paper cannot cover. It might be used on the training process as well, since the wizard's steps explain on a broad manner the interface options and even the application manual is large enough on directions …

… The variable among simulations was the model for the ODT enabled, for the data nets (as shown in the figure 10). In the figure 11 the red color points out the values out of range, in the current case the overshoot and undershoot above the 400mV.

TABLE I. SIMULATION RESULTS FOR VARIOUS ODT MODELS

DM_ODT enabled_models	pass	overshoot margin (mv)	undershoot margin (mv)
DM_INPUT_1066	NO	-58.3	-135
DM_INPUT_1600	NO	-58.3	-135
DM_INPUT_1866	NO	-58.3	-135
DM_ODT20_1066	YES	400	400
DM_ODT20_1600	YES	400	400
DM_ODT20_1866	YES	400	400
DM_ODT30_1066	YES	400	400
DM_ODT30_1600	YES	400	400
DM_ODT30_1866	YES	400	400
DM_ODT40_1066	YES	400	400
DM_ODT40_1600	YES	400	400
DM_ODT40_1866	YES	400	400
DM_ODT60_1066	YES	400	400
DM_ODT60_1600	YES	400	400
DM_ODT60_1866	YES	400	400
DM_ODT120_1066	YES	245.8	196.1
DM_ODT120_1600	YES	245.8	196.1
DM_ODT120_1866	YES	245.8	196.1

… results of using for the ODT the model DM_INPUT_1066, are depicted.

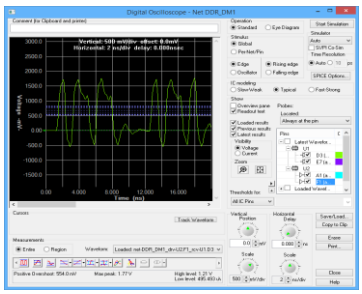

Fig. 1. Positive overshoot calculated for the net DDR_DM1

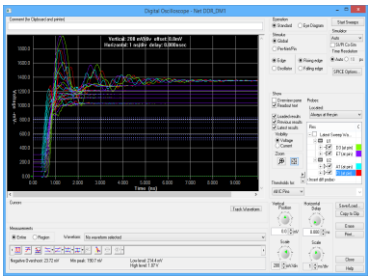

Fig. 2. Sweeping analysis for 18 ODT models

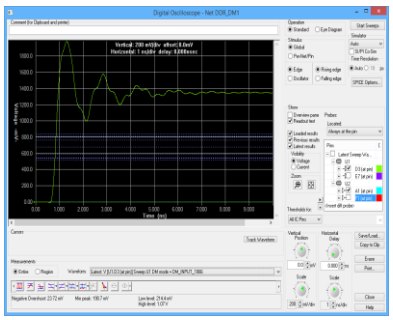

Fig. 3. The waveform at the pin U1.D3 (the ODT model DM_INPUT1066 used)

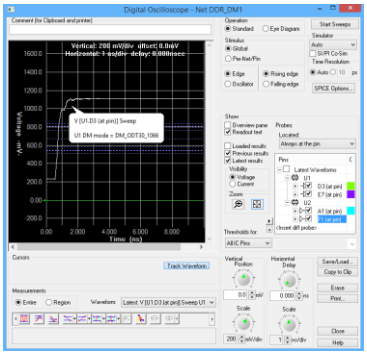

Fig. 4. The waveform at the pin U1.D3 for the ODT model DM_ODT30_1066 used (correct result)

HyperLynx DRC, as unique tool on the marked, has several advantages such as the functional physical verifications that might be run on the printed circuit boards projects, the intellectual property that includes by the verification rules that can be defined and used for any other printed circuit board project and even more, no prior simulation knowledge in analysis and simulation is necessary. That is why this solution is addressable by any person with minimal technical background in printed circuit boards. The hardcoded simulation rules help the user to easily figure out the trouble on the board that can cause signal integrity, power integrity and electromagnetic interference and compliance issues.