… **HyperLynx DRC** developed from the Company **Mentor Graphics** … is able to run both geometrical or electrical rules as well as high-speed specific rules … The interface is easy to use, intuitive. The analysis process includes several steps steps such as:

- design import – the import accepts several formats including ODB++, pcb, xml or, the one integrated with the printed circuit board solutions from **Mentor Graphics**, cce, an intelligent format;
- design analysis setup throughout an assistant interface - an wizard that allow you to set the unit for the length or for the electrical parameters like current, voltage, capacitance, resistance and so on. The default values for missing net and stackup definition, the project paths, the component models, for the electrical nets and eventually the rules that will be run after the setup process,
- the analysis itself – as long as the user goes through the wizard, the final step could be to run the analysis or just to end the setup process in order to position to he main working area

… very much intellectual property from the printed circuit board market was implemented on it, under rules format. The user has nothing else to do than to run the simulation after very few setup steps. There are rules hard coded, based on the information gathered from the industry. … if any particular rule is not in the … list, the user is able to define (based on a certain level of licensing) custom rules. The rules can be reused for any project, no need to redefine them for each individual design. Numeric constraints mapped to the simulating parameters

For the current project we activated some rules as following:

- EMI (electromagnetic integrity) – Metal Island, Net Crossing Gaps and VIA stub Length
- PI (power integrity) – Decouping Capacitor Placementand Decoupling Capacitor Order
- SI (signal integrity) – Crosstalk Coupling and Diff Pair

For the project we applied the analysis rules, we obtained errors for most of the rules we activated. There are 6 crosstalk coupling errors, 2 trace leaves reference plane, 231 crossing split errors, 2 differential pair, 21 isolated metal and 657 Via stub length violation.

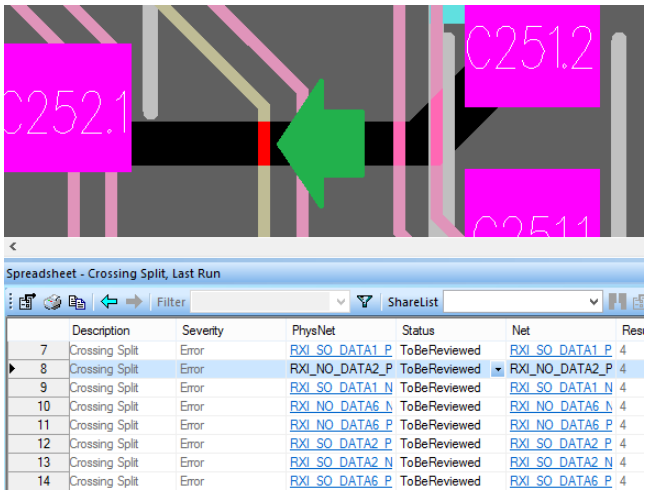

Fig. 1. Crossing split errors

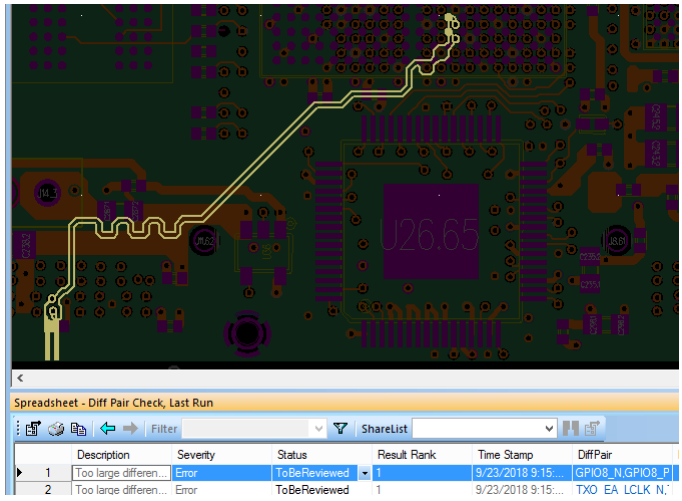

Fig. 2 Differential pairs errors

For inspection by other team member on different geographical site, the results were exported and sent out by email. Then the errors were negotiated with the hardware designer.

HyperLynx DRC, as unique tool on the marked, has several advantages such as the functional physical verifications that might be run on the printed circuit boards projects, the intellectual property that includes by the verification rules that can be defined and used for any other printed circuit board project and even more, no prior simulation knowledge in analysis and simulation is necessary. That is why this solution is addressable by any person with minimal technical background in printed circuit boards. The hardcoded simulation rules help the user to easily figure out the trouble on the board that can cause signal integrity, power integrity and electromagnetic interference and compliance issues.