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Jan 01 | 2019 - HDL Frührschoppen

INVITATION - HDL "Frührschoppen" - free of charge



First of all we wish you a Happy New Year and immediately start 2019 with an invitation.

During our HDL "Frührschoppen" we want to stimulate your grey cells and reward you with a nice lunch, during which you can discuss what you have learned even further.

This time we will concentrate on an interesting subject: **"Exhaustive automated formal solutions for FPGA verification challenges"**.

We were able to win Stefan Bauer, one of Mentor's verification experts, for this event. He will introduce formal techniques to verify clock domain crossing issues, and to find bugs due to common RTL coding errors. Furthermore you will learn how to use Mentor's formal apps within the FPGA vendor tools like Xilinx Vivado or Intel Quartus.

And so we would like to invite you to join us in:

▶ **5. February 2019 | Stuttgart**
Stuttgarter Schlachthof

[Info & RSVP](#)

▶ **6. February 2019 | Düsseldorf**
Alter Bahnhof Oberkassel


[Info & RSVP](#)

Don't forget to find out about the interesting FPGA design and verification trainings we can offer, as well as courses on other topics. In addition to the open workshop dates we also offer on-line and in-house training.

Please contact us on +49 (0) 2151 / 95301-0 or by email at education@trias-mikro.de.

Best regards
Team TRIAS

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