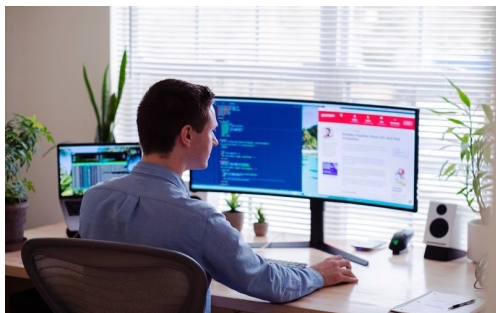




September | 2020 - Online Course

### SYSTEMVERILOG – ADVANCED VERIFICATION FOR FPGA DESIGN

19. - 21.10.2020



As you surely know, training is and will remain an important topic - especially at the moment. Therefore we would like to inform you about our online course **SystemVerilog - Advanced Verification for FPGA Design**, which is taking place from 19.-21. October 2020.

In this course you will be trained in SystemVerilog in connection with innovative verification methods "Assertion Based Verification", "Constrained-Random-Generation" and "Functional Coverage". Participants will learn how these powerful verification methods are used to speed up verification and track verification progress, as well as how these methodologies can be applied to the verification of VHDL designs.

Due to the secure **online** format, this course is ideal for participation, whether working in the home office or workstation in the office. There are still places available, so register now:

▶ [SystemVerilog – "Advanced Verification" für FPGA Design](#)

Register



In addition to these course dates, we also offer in-house training on these and other topics on request.

Please do not hesitate to contact us on +49 (0) 2151 / 95301-0 or simply by email [[LINK mailto='education@trias-mikro.de '](mailto:education@trias-mikro.de)] [education@trias-mikro.de](mailto:education@trias-mikro.de) [/ [LINK](#)].

Best regards and stay safe!

Pia Pacovsky  
TRIAS mikroelektronik GmbH

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