



February | 2021

ONLINE TRAINING: Accelerating FPGA VHDL Verification and introducing UVVM



You are surely following the FPGA verification news and know that the modern verification method **UVVM** (Universal VHDL Verification Methodology) – has become the **No. 1 of the world's leading VHDL-FPGA verification methods**. This course, by Espen Tallaksen, contains a general introduction to UVVM, the verification method that shows the fastest growth independent of HDL.

On average almost half the time of an FPGA project is spent on verification. It is possible to reduce this time significantly, and even greater savings can be achieved with minor adjustments.

In this online course with **ESPEN TALLAKSEN**, the main architect of UVVM, theory alternates with practical examples and hands-on tutorials. Take this opportunity to get to know the Universal VHDL Verification Methodology (UVVM) and learn how you can reduce development time while improving quality.

The course is definitely for you if you want to rethink your testbench methodology because your current approach has reached its limits, or if you are generally looking for a VHDL testbench library with which a complete, well-structured testbench can be assembled from individual components.

The only requirement for participation in this course is knowledge of VHDL.

▶ **Accelerating FPGA VHDL Verification and introducing UVVM**
19. - 23. April 2021


[more information](#)


In addition to this course, we offer a wide range of online training courses on a variety of topics. [Check it out yourself](#) or contact us.

Best regards and stay safe

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