12|2021

TRIAS TRAINING CENTER

ACCELERATING FPGA VHDL VERIFICATION AND INTRODUCING UVVM

DESCRIPTION

Efficiency and quality is all a question of overview, readability, extensibility, maintainability and reuse, - and a good architecture is the answer. This applies for both Design and Verification.
This course contains a general introduction to modern verification methodology and to UVVM (Universal VHDL Verification Methodology) – the world-wide #1 VHDL-FPGA verification methodology, and also the fastest growing verification methodology independent of HDL.
On average half the development time for an FPGA is spent on verification. It is possible to significantly reduce this time, and major reductions can be accomplished with minor adjustments. In this course you will learn how to reduce development time and at the same time improve the quality.
The course will concentrate on FPGA verification and how a well structured testbench is constructed. Theory alternates with practical examples, as well as hands-on tutorials. It also covers important topics such as coverage, Bus Functional Models (BFM), debugging and randomization.
After the course, participants will know how to structure an FPGA verification platform, how to implement their testbenches, and how to write test sequencers, which can be understood by software and hardware developers. Participants will also learn how to use the complete VHDL-based UVVM verification platform within their own organization

AGENDA

- Making a simple VHDL testbench step-by-step
- Using procedures and making good BFMs
- Applying logs, alerts, value and stability checkers, awaits, and more
- Making an advanced VHDL testbench step-by-step
- Assertions, randomization, constrained random, coverage, debuggers, monitors
- Verification components and testbench architecture for advanced verification
- Making testbenches as simple as possible – adapting to the DUT complexity
- Structuring, Debugging, Overview, Maintainability, Extendibility
- Examples and labs using UVVM

TARGET GROUP
FPGA and Digital ASIC Designer

PREREQUISITES
Knowledge of VHDL

DURATION
3 days

LANGUAGE
English

COURSE TARGETS
- Structure an FPGA-verification platform
- Improvement of your general working methodology
- Set up and use of UVVM framework
- Develop and use Bus Functional Models and VHDL Verification Components
- Reuse and modification of BFMs and VVCs with minimum effort
- Significant reduction of verification time

COSTS
€ 2.100,00 per participant*

www.trias-mikro.com

**including training materials, lunch and refreshments*

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TRAINER

Espen Tallaksen

is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement.

One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He is giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

FURTHER COURSES

Accelerating FPGA and Digital ASIC Design

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