ACCELERATING FPGA AND DIGITAL ASIC DESIGN

DESCRIPTION

Digital design for FPGAs and ASICs has a huge improvement potential with respect to development time and product quality.

A lot of time is wasted on inefficient design and lack of awareness and knowledge of the most critical digital design issues. This also seriously affects the quality of the end product. The really good thing is that this huge improvement potential can be realised just by making a few important changes to the way we design.

There will be a few examples on quite common bad approaches, and more examples on good approaches for architecture, Clock Domain Crossing (CDC), Coding, Reuse, etc.. Almost all examples are independent from both technology (FPGA/ASIC) and language (VHDL/Verilog /SystemVerilog).

The course is intended for FPGA designers and Digital ASIC designers, who wants to work smarter and more efficiently - and design products with higher quality.

AGENDA

- Making a simple VHDL testbench step-by-step
- Using procedures and making good BFMs
- Applying logs, alerts, value and stability checkers, awaits, etc.
- Making an advanced VHDL testbench step-by-step
- Assertions, randomization, constrained random, coverage, debuggers, monitors
- Verification components and testbench architecture for advanced verification
- Making testbenches as simple as possible – adapting to the DUT complexity
- Structuring, Debugging, Overview, Maintainability, Extendibility
- Examples and labs using Universal VHDL Verification Methodology (UVVM)

TARGET GROUP

FPGA- and Digital-ASIC Designer

PREREQUISITES

Knowledge of FPGA Design or Digital ASIC Design

DURATION

2 days

LANGUAGE

Englisch

COURSE TARGETS

- Design Structure
- Clock Domain Crossing (CDC)
- Coding
- Maintainability
- Readability
- Pitfalls and Reuse
- Quality Assurance

COSTS

€ 1.450,00 per participant*

www.trias-mikro.com

**including training materials, lunch and refreshments*

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TRAINER

Espen Tallaksen

is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement.

One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He is giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

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FURTHER COURSES

- Accelerating FPGA VHDL Verification