08|2018

TRIAS TRAINING CENTER

VERILOG FOR VHDL USER

DESCRIPTION

This course provides an overview of Verilog for VHDL users and is a brief introduction to Verilog. It is targeted at designers with experience in VHDL, and it focuses on the techniques needed for RTL and testbench design.

As designs grow more complex and design cycles shrink, design teams resort more and more often to the use of Intellectual Property, to design reuse and to collaboration with other remote teams. This means engineers must become „language neutral" - that is have solid understanding of both VHDL and Verilog and their associated design techniques.

Our hands-on course is a fast and effective method for experienced VHDL users to understand the differences, as well as the similarities between VHDL and Verilog as well as to master those Verilog-specific issues that tend to create hard-to-detect problems (e.g. no blocking assignments).

AGENDA

- Overview
- A bit of history
- RTL
  - Interface & Hierarchy
  - Signals
  - Operators
  - Parameters
  - Tasks and Functions
  - Mixed Language design
  - etc.
- Testbench
  - Procedural continuous assignment
  - System Tasks
  - etc.
- Advanced
  - Compiler directives: `uselib, `reset_all
  - Verilog libraries
  - Gate-level simulation

TARGET GROUP

Engineers with VHLD experience, who intend to design with Verilog. Engineers who want to extend their Verilog knowledge

PREREQUISITES

Digital Hardware Design basic knowledge and good VHDL knowledge. No basic knowledge required in Verilog.

DURATION

2 days

LANGUAGES

English or German

COURSE TARGETS

- Understand the concepts of Verilog and how they differ from VHDL
- Understand the Verilog-specific techniques for RTL design
- Learn how to avoid Verilog pitfalls

COSTS

€ 1.400,00 per participant*

www.trias-mikro.de

**Including training materials, lunch and refreshments*

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TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikro-elektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.

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ADDITIONAL COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- UVM Made Easy for FPGA Designers