Calibre xACT

Next-generation parasitic extraction

Benefits

- High extraction accuracy
- Attofarad accuracy for digital, custom, analog, and memory designs
- Advanced device modeling (including FinFET) integrated with Calibre nmLVS
- Deterministic, repeatable results
- Fast, scalable performance
- 10X the performance of previous solutions handles multi-million instance designs
- Multi-threaded, distributed processing architecture

Advanced nanometer design

Successive generations of foundry process technologies enable ever-increasing design density, performance and power savings, but also present designers with burgeoning challenges. For example, innovative new process features such as FinFET transistors represent a paradigm shift for low-power design, and require a corresponding leap in the performance and accuracy from electronic design software. Calibre® extraction tools are continually improved to accurately and efficiently model the physical effects of these new process technologies, and are qualified by silicon manufacturers under extremely stringent accuracy criteria. The Calibre xACT™ parasitic extraction solution represents the state-of-the-art in this continuing development. It is a high-performance, high-accuracy parasitic extraction tool that gives designers confidence that their performance and integration goals will be fully realized in silicon.
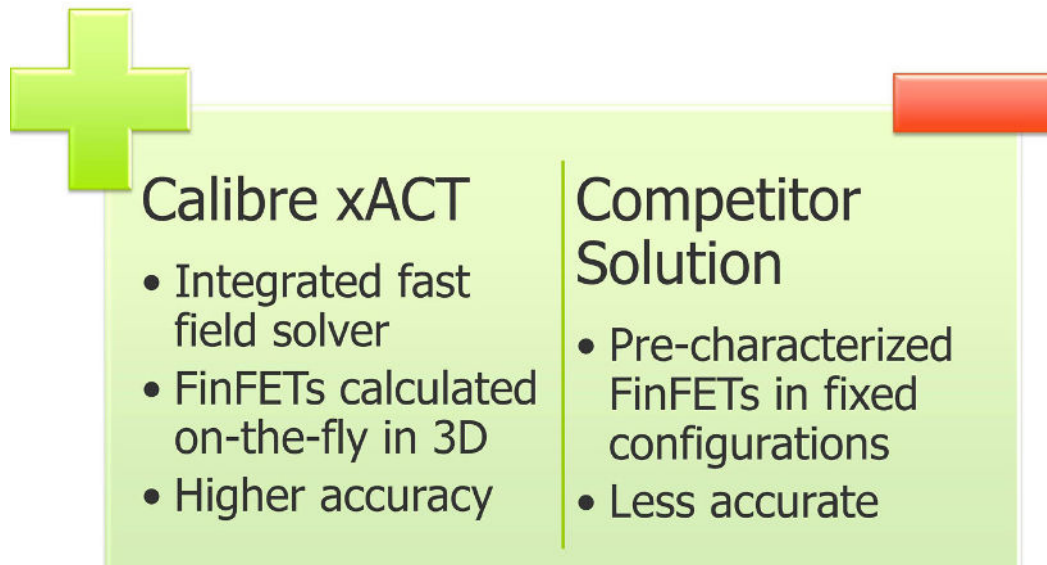
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Benefits *continued*

- Simultaneous multi-corner extraction; results match singlecorner runs

- Support for digital, analog and custom designs

- Foundry rule decks for all major manufacturers
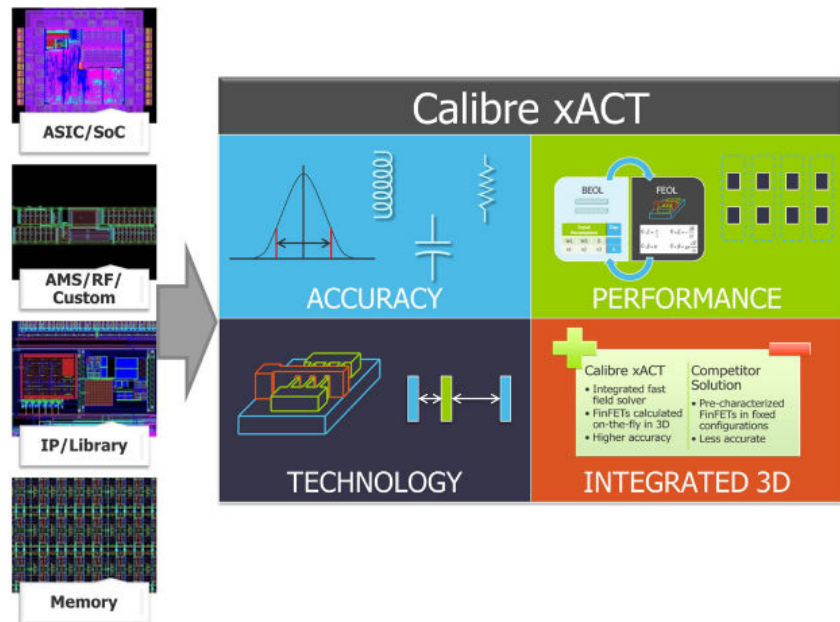
The Calibre xACT platform quickly and accurately, extracts parasitic capacitance, resistance and inductance for a variety of IC design styles, from digital to custom analog and RF.

The Calibre xACT platform is architected from the top-down to accurately model physical and electrical effects resulting from the complex structures and manufacturing processes employed at advanced nodes. Using net-based parallelism with multi-CPU processing, the Calibre xACT tool can quickly and accurately generate parasitic capacitance, resistance and inductance netlists for diverse IC design styles, from digital to custom analog and RF, providing the data needed for post-layout analysis. With an integrated fast 3D field solver, the Calibre xACT tool provides attofarad-accurate results for dynamic analog circuit simulation, while also delivering the performance and capacity needed for multimillion instance digital designs. The Calibre xACT platform uses foundry-qualified rule decks in the Calibre SVRF language, and is interoperable with the Calibre nmLVS™ tool and with industry-leading design implementation platforms. The Calibre xACT platform delivers the best combination of accuracy and turnaround time for leading-edge node designs, automatically optimized for the particular IC application and size, process technology, and downstream analysis flow.

Calibre xACT

- Integrated fast field solver
- FinFETs calculated on-the-fly in 3D
- Higher accuracy

Competitor Solution

- Pre-characterized FinFETs in fixed configurations
- Less accurate

The Calibre xACT platform calculates FinFET parameters on-the-fly using its integrated 3D field solver. The product does not require precharacterized FinFET layouts. Using a very fast field solver to generate on-the-fly patterns based on the device structures in the design enables the highest possible accuracy.

Advanced process node extraction

It is paramount to accurately capture the parasitic resistance and capacitance within FinFET devices, as well as interactions between devices. Some foundries use floating devices between the designed FinFETs, so it is important to capture coupling to the floating devices and between the main active devices. Parasitic resistance is also important— as the fin channel and the source drain regions narrow, increased source-drain resistance degrades device performance.

Either the parasitic extraction tool or the simulation device model can calculate parasitic capacitance and resistance within (and between) FinFETs. The trend for smaller nodes is to place the modeling burden on the parasitic extraction tool because it can take layout-dependent effects into consideration. The Calibre xACT platform automatically selects the appropriate combination of

extraction techniques for front end of line (FEOL) and back end of line (BEOL) geometries to meet foundry and customer needs for accuracy, while still maintaining the through-put required to meet evershrinking time-to-market windows. The Calibre xACT platform is integrated with the Calibre nmLVS tool to ensure that no effects are double-counted or missed in the boundary between the extraction tool and the device model.

Integrated fast field solver

the Calibre xACT platform incorporates a fully-integrated fast field solver built on advanced computational electromagnetic methods to accurately calculate device and interconnect parasitics. Unlike other field solvers that use statistical methods, the Calibre xACT field solver employs deterministic techniques that produce reliable, rotationallyinvariant total and coupling capacitance results, while providing superior, scalable performance.

Multi-patterning

Multi-patterning uses multiple masks per layer to print geometries that are too small to resolve accurately with one mask. Any misalignment of these masks during manufacturing impacts the predictability of parasitic capacitance by increasing or decreasing the distance between features on multi-patterning layers.

The Calibre xACT platform enables designers to characterize potential misalignment by performing simulations with multi-patterning corners. This simulation ensures that the circuit is sufficiently robust to contend with any resulting manufacturing variation.

Digital design

The Calibre xACT platform provides fast, full-chip, signoffquality parasitic extraction for cell-based digital design flows. It employs a combination of efficient algorithms to deliver very fast single-CPU performance. I ts highly-scalable multi-threaded, multi-CPU architecture ensures that digital designers have the performance and capacity they need to extract the largest chips while meeting their time-to-market schedules.

Multiple corner extraction

The Calibre xACT platform incorporates a fast and efficient implementation of simultaneous multi-corner extraction that provides stable, deterministic results. Each additional corner typically generates only a 15-20% performance overhead with no loss in accuracy. This is in contrast to tools based on stochastic methods, which typically require several days for multi-corner extraction and suffer from accuracy drift between multi-corner and single corner results. the Calibre xACT solution makes it possible to turn around multi-million instance full-chip designs with multiple process, double patterning, and temperature corners in a single workday.

Net-based parallelism and multi-CPU processing

The Calibre xACT platform achieves fast performance and scalability with a massively parallel architecture using netbased parallelism, achieving nearly ideal linear scaling. With the Calibre xACT, solution each net is processed intact instead of using the typical tiling method, which cuts the net into many pieces. Each complete net is then computed on a single CPU rather than being distributed across multiple CPUs. This "net-based parallelism" approach eliminates boundary and halo effects on accuracy, and provides better scalability than tiling, especially on symmetric multiprocessing (SMP) machines. Net-based parallelism also eliminates variance in the accuracy of results that occurs with tiling when the number CPUs changes.

Metal fill and GDS macro file processing

The escalating amount of fill data associated with large nanometer designs presents a considerable burden to parasitic extraction. Extraction tools must read and process gigabytes of data in order to accurately model the density and parasitic capacitances of wires adjacent to fill patterns. Processing this data quickly and producing a compact fill model is essential to maintaining throughput and managing memory usage of extraction tools. Large GDSII and OASIS macros pose the same problem of how to maintain accuracy with little or no performance compromise.

To address these challenges, the Calibre xACT platform takes advantage of the hyper-efficient geometry processing that Calibre nmDRC™ users have enjoyed for many years. The Calibre xACT platform maintains fast throughput and high accuracy for the largest nanometer designs, even when gigabytes of fill and macro data are incorporated in the extraction run.

Timing sign-off

Static timing analysis is a significant bottleneck for tapeout of digital designs. The problem is compounded by the increase in the number of process and multi-patterning corners required at 16nm and below. Often, digital designers are forced to limit their timing analysis runs to a few well-chosen corners, increasing the risk of missing a critical corner combination.

Designers can leverage the simultaneous multi-corner processing capability of the Calibre xACT platform to generate additional netlists and validate their assumptions about corner scaling, with minimal execution time overhead. The Calibre xACT solution is also tolerant of faults such as shorts and opens, so digital designers can produce extraction results sooner in the design flow and get much needed early feedback on the timing effects of their place-and-route strategies.

Analog/mixed-signal and custom design

The Calibre xACT architecture delivers unprecedented accuracy for extraction of advanced node geometries, such as finFET transistors. It automatically extracts with more precision in areas where higher accuracy is required, while providing extremely fast extraction for upper metal layers. It also provides optimal results for micro-electromechanical systems (MEMs), silicon photonics, and RF designs with minimal designer setup effort.

The Calibre xACT selective net processing capability tailors the amount of data for simulation by allowing designers to select the parasitic model they want for each net. Designers can select distributed RCC (with coupling capacitance), RC (no coupling capacitance), C or R, on a net-by-net basis. Designers can also control extraction by layer. For example, to reduce simulation time while taking into account the parasitic effects for large power and ground nets, designers can extract VDD and VSS nets including only via resistance, and excluding metal layer resistance,

since vias contribute the most resistance to the power/ground net. This enables faster simulation while still maintaining accurate design margins.

The Calibre xACT platform uses reduction techniques to control the number of parasitic elements that are included in the netlist. Its default reduction settings are optimized for both analog and digital designs, to produce compact and accurate netlists for post layout simulation and timing analysis. Designers can also fine tune global reduction settings to control the level of accuracy and netlist size as needed.

Inductance extraction

The Calibre xACT platform enables fast and accurate full-chip extraction of inductance effects in analog, RF and digital designs. Designers can restrict inductance extraction to selected sensitive nets, such as RF or clock tree nets to minimize overhead.

Tool integration

The Calibre xACT platform is integrated with the Calibre nmLVS tool for complete transistor-level modeling of custom and cell-based designs. It is also integrated with a wide variety of 3rd-party design environments and formats to ensure compatibility with design and post-layout simulation and analysis flows. The Calibre RVE™ results viewing environment makes it easy for designers to visualize parasitic results and make corrections in the layout editing environment. For users familiar with the Calibre use model, adoption and implementation is fast and simple, allowing design teams to reach the desired results quickly.

Sign-off confidence

Rule files for the Calibre xACT platform are available from all major foundries and for all popular processes, including TSMC 16nm and Samsung 14nm.