HDL Simulation

ModelSim

Verification and simulation tools from Siemens Digital Industries Software

Benefits

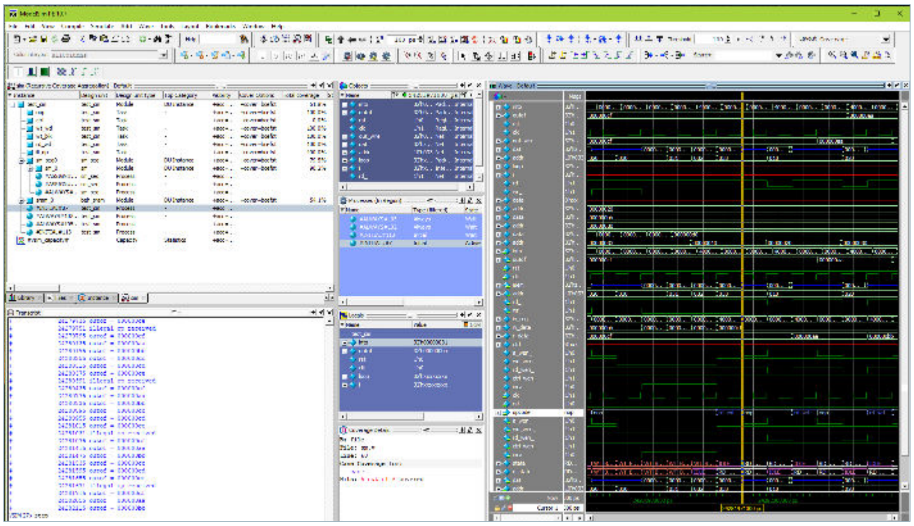
- Native compiled, single kernel simulator technology
- VHDL, Verilog, and SystemVerilog design constructs
- Intelligent, easy-to-use GUI with Tcl interface
- Integrated project management, source code templates, and wizards
- Wave viewing and comparison; objects, watch, and memory windows increase debug productivity
- Code coverage
- Standard support for Xilinx® SecureIP
- SystemC option available
- SVA and PSL assertions

Sophisticated FPGA Verification

ModelSim® packs an unprecedented level of verification capabilities in a cost-effective HDL simulation solution. In addition to supporting standard HDLs, ModelSim increases design quality and debug productivity.

ModelSim's award-winning single kernel simulator (SKS) technology enables transparent mixing of VHDL and Verilog in one design. Its architecture allows platform-independent compile with the outstanding performance of native compiled code. The graphical user interface is powerful, consistent, and intuitive. All windows update automatically following activity in any other window. For example, selecting a design region in the structure window automatically updates the source, signals, process, and variables windows. You can edit, recompile, and re-simulate without leaving the ModelSim environment. All user interface operations can be scripted and simulations can run in batch or interactive modes.

ModelSim simulates behavioral, RTL, and gate-level code, including VHDL VITAL and Verilog gate libraries, with timing provided by the standard delay format (SDF).



ModelSim offers the most verification capabilities in its class.

HDL Simulation – ModelSim

A More Intelligent GUI

An intelligently engineered GUI makes efficient use of desktop real estate. ModelSim offers a highly intuitive arrangement of interactive graphical elements (windows, toolbars, menus, etc.), making it easy to view and access the many powerful capabilities of ModelSim. The result is a feature-rich GUI that is easy to use and quickly mastered. ModelSim redefined openness in simulation by incorporating the Tcl user interface into its HDL simulator. Tcl is a simple but powerful scripting language for controlling and extending applications.

The ModelSim GUI delivers highly productive design debug and analysis capabilities as well as project and file management.

Memory Window

The memory window allows intuitive and flexible viewing and debugging of design memories.

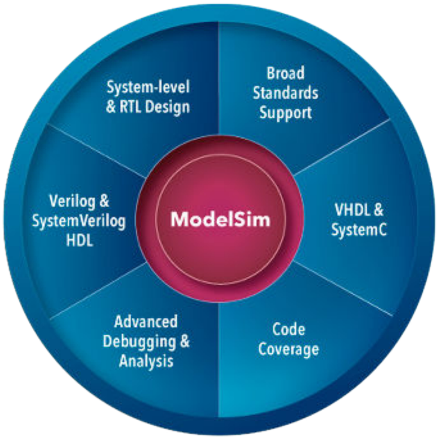
VHDL and Verilog memories are auto-extracted from the source and viewed in the GUI, allowing powerful search, fill, edit, load, and save functionality. The Memory window supports pre-loading memories from a file or using constant, random, and computed values, saving the time-consuming step of initializing sections of testbenches just to load memories. All functions are available via the command line, allowing their use in scripting.

Waveform and Results Viewing

ModelSim provides a high performance, full-featured Wave window. The Wave window provides cursors for marking interesting points in time and measuring the time distance between cursors. Wave window contents can be formatted flexibly through powerful virtual signal definitions and grouping.

Waveform comparisons are easily performed between two simulation results. Timing differences between RTL and gate-level simulation results are easily handled through user-specified time-filtering capabilities.

ModelSim provides a unique WLF management utility (aka WLFMAN) that allows the manipulation of WLF result files, enabling you to specify the amount of information to record to a WLF file or to subset an existing WLF file based on signals or time. The WLFMAN utility allows efficient management of disk space and post-simulation debug efficiency.


ModelSim
System-level & RTL Design
Broad Standards Support
VHDL & SystemC
Code Coverage
Advanced Debugging & Analysis
Verilog & SystemVerilog HDL

Source Window Templates & Wizards

VHDL and Verilog templates and wizards allow you to quickly develop HDL code without having to remember the exact language syntax. All the language constructs are available with a click of a mouse. Easy-to-use wizards step you through creation of more complex HDL blocks. The wizards show how to create parameterizable logic blocks, testbench stimuli, and design objects. The source window templates and wizards benefit both novice and advanced HDL developers with time-saving shortcuts.

Project Manager

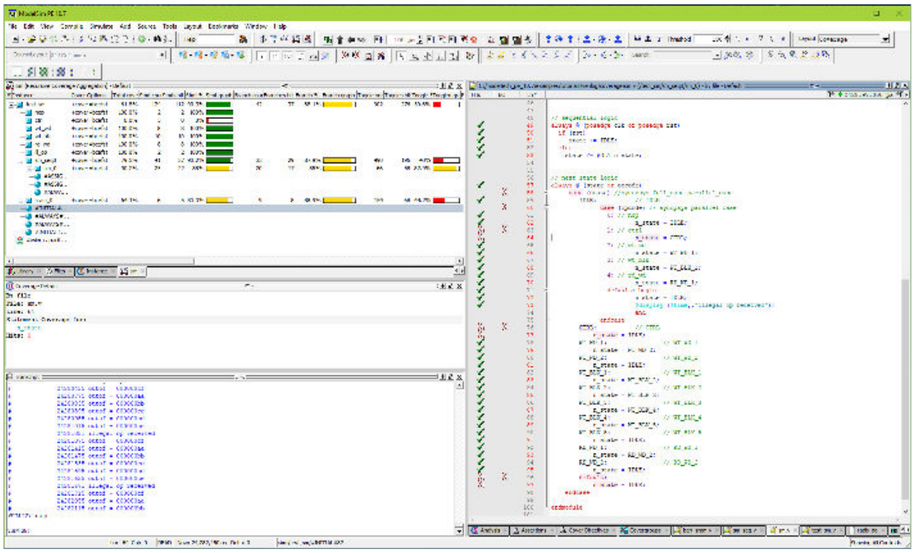
The project manager greatly reduces the time it takes to organize files and libraries. As you compile and simulate, the project manager stores the unique settings of each individual project, allowing you to restart the simulator right where you left off. Simulation properties allow you to easily re-simulate with pre-configured parameters.

Code Coverage

Design verification completeness can be measured through code coverage. ModelSim supports statement, expression, condition, toggle, and FSM coverage. Code coverage metrics are automatically derived from the HDL source. As many design blocks are created to be configurable and reusable and not all metrics are valuable, code coverage metrics can be flexibly managed with source code pragmas and exclusions specified in the code coverage browser.

Assertion Based Verification

ModelSim delivers a comprehensive, standards-based assertion based verification (ABV) solution, offering the choice of SystemVerilog Assertions (SVA), Property Specification Language (PSL), or both.



Using integrated code coverage, ModelSim tracks how much of the design has been tested.

Powerful, Cost-Effective Simulation

ModelSim delivers a powerful simulation solution ideally suited for the verification of small and medium sized FPGA designs; especially designs with complex, mission critical functionality.

Platform Support

ModelSim is supported on 32/64-bit Windows 10, Linux RHEL6 and RHEL7, and Linux SLES 11 and SLES 12 based platforms. When running on a 64-bit system, ModelSim runs in 32-bit mode.

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