

# Questa Verification IP

## An integral part of the Enterprise Verification Platform from Siemens Digital Industries Software

### Benefits

- Consistent UVM architecture
- Easy-to-use EZ-VIP API
- Fast bring up
- Responsive, expert support 24/7
- Supported on all simulators
- Comprehensive test suite and compliance tests
- Complete verification plan, protocol coverage, and checking
- Intuitive transaction-level debug
- High-quality, mature VIP validated against commonly used design IP

### Fastest time to verification sign-off

Siemens EDA Questa® Verification IP (QVIP) integrates seamlessly into all advanced verification environments on any simulator. With a consistent and easy-to-use UVM architecture across all protocols, QVIP ensures maximum productivity and flexibility for the verification of block level, subsystem, and SoC designs.

Today's designs rely heavily on a growing variety of complex industry standard interface protocols. QVIP enables engineers to effectively deal with this complexity, improves quality, and reduces schedule time by building Siemens EDA, a part of Siemens Digital Industries Software, protocol and methodology expertise into a library of reusable components that support many industry standard interfaces. This frees engineers from spending time developing BFM, verification components, or VIP, so they can focus on the unique and high-value aspects of their designs.

Serial	AMBA®	Display	Ethernet			DRAM	
QSPI	CHI	HDMI 2.1	1G Base T1	100M Base T1	10M Base T1	DDR5	
SPI	AMBA LPI	HDMI 2.0	200/400G	100G	12/50G	LPDR4	
SPI 4.2	AXI5	HDMI 1.4	40G	10G	2.5/5G	DDR4	
Smartcard	AXI4	DisplayPort	1G	1000M	10M	LPDDR3	
I2C	AXI3	eDP	QSGMII	USXGMII	USGMII	DDR3	
I3C	AHB5	V-by-One	RGMII	MLG	Preemption	LPDDR2	
I2S	AHB	CEC	Interlaken	MACSEC		DDR2	
JTAG	APB3	HDCP					
UART							
SMBUS							
	Flash						
	SDCard 6.0	eMMC 5.1					
	SDIO 4.1	ONFI 4.1					
HBM	Toggle	UFS					
HBM2E	Parallel NOR	Serial NOR					
HBM2	Serial NAND						
DFI							
			Mil-Aero		PCIe®	NVMe	USB
			Spacewire	PCIe 5.0	NoF 1.0	UB 3.2	
			153b	PCIe 4.0	NVMe 1.4	USB TypeC	
			PCI	PCIe 3.1	NVMe 1.3	USB PD	
			SRIO	PCIe 2.1	NVMe 1.2	USB 3.1	
					NVMe 1.1	USB 3.0	
						USB 2.0	
			Other				
			Contact Mentor for additional verification IP components not listed here				

Questa Verification IP library.

# Questa Verification IP

## Large library of protocols and memory models

QVIP supports a large library of industry-standard protocol and memory interfaces and devices. It includes standard SystemVerilog UVM components using a consistent, common architecture that allows rapid deployment and sharing of multiple protocols and memory models within a verification team. Test plans, compliance tests, test sequences, and protocol coverage are all included as SystemVerilog and XML source code, allowing easy reuse, extension, and debug. All QVIP components include a comprehensive set of protocol checks, error injection, and debug capabilities.

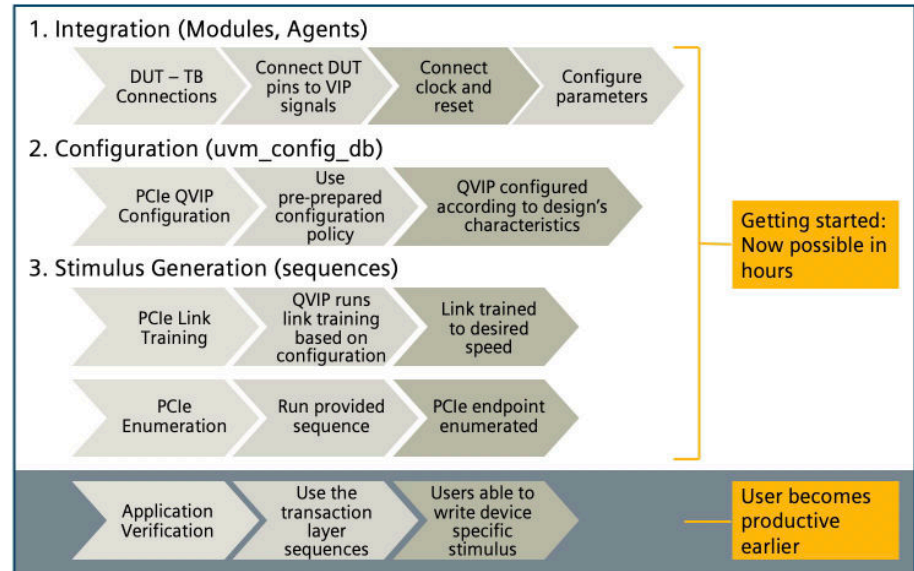
## EZ-VIP: Architected for rapid productivity

EZ-VIP APIs and quick starter kits take care of the tedious connection, configuration, and set up tasks, so engineers can start writing tests using QVIP within a day, even for complex serial protocols, such as PCI Express and USB.

- Reusable protocol test plans linked to supplied protocol coverage
- Complete protocol checks and test suites achieve 100 percent protocol coverage to verify protocol compliance
- Comprehensive VIP built using advanced methodologies for fastest time to verification sign-off

## An integral part of the enterprise verification platform

Questa Verification IP is a key component of the Enterprise Verification Platform (EVP). Complete VIP components reduce bring up time and enable rapid coverage closure. Common APIs and methodologies enable tests and testbenches to be moved from one verification engine to another. As an integral part of EVP, QVIP can be used with a combination of shared databases, debug applications, and analysis tools, allowing users to choose the best tool for different tasks within a single, highly productive verification flow.



Three Steps to Productivity with VIP: Integrate > Configure > Generate Stimulus > Verify Product

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