DIGITAL INDUSTRIES SOFTWARE

Calibre nmDRC

Early design physical verification

Features

- Automatic intelligent DRC subset selection
- Allows designers to focus on systemic errors pertinent to early design stages
- Allows designers to check top-level routing while ignoring cell details
- Separates integration and routing errors associated with assembly from immature/dirty block violations
- Uses foundry DRC process design kits “as-is”
- Multiple analysis options support data-driven and visual debugging

Design teams face continuous pressure to reduce time to market. In an effort to accelerate design closure, it is increasingly common to see design teams performing design rule checking (DRC) verification across blocks, macros, and full chip layouts in parallel while many components are still immature, resulting in long runtimes and challenging debug cycles.

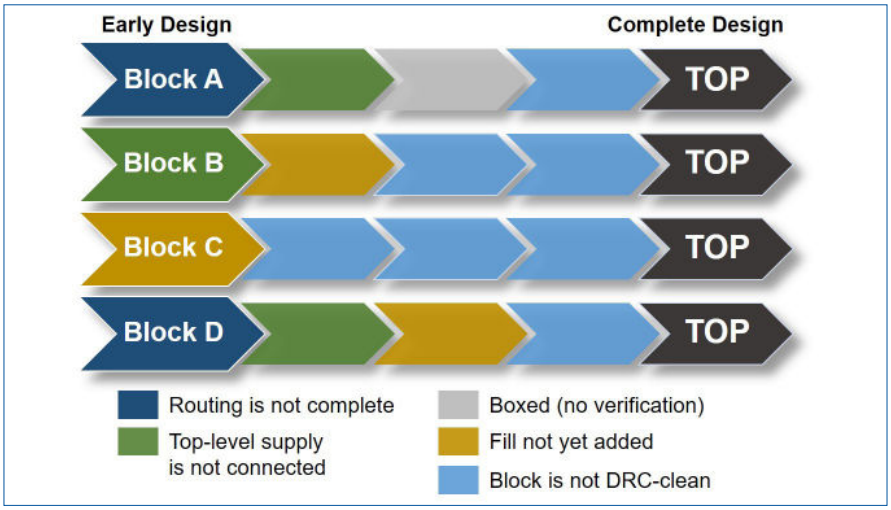
Calibre® nmDRC-Recon™ early DRC verification enables verification teams to perform a rapid reconnaissance of “dirty” blocks and incomplete designs, using selective DRC to methodically find and quickly fix targeted DRC errors earlier and faster. The Calibre nmDRC-Recon tool speeds design closure by using innovative functionalities that enable designers to focus only on high-impact DRC issues.

Automatic check selection

During early design phases, unfinished blocks contain huge numbers of DRC violations, including many systemic DRC issues such as off-grid block placement, or routing in IP on a reserved routing layer. Using intelligent heuristics, the Calibre nmDRC-Recon technology automatically deselects checks that are not relevant to the current development phase. It decides which checks to omit based on the check type and the number of operations executed for the check, with the goal of achieving fast runtimes while still providing appropriate design rule coverage. Designers can also manually control the deselection of checks/categories, if desired.

Benefits

- Quickly identifies floorplan and sub-chip integration issues that are more meaningful to the targeted implementation stage.
- Fast, in-depth error visualization and analysis
- Accelerates design closure turnaround time



Running targeted verification flows in parallel with block development reduces overall DRC iterations and time.

Targeted block verification

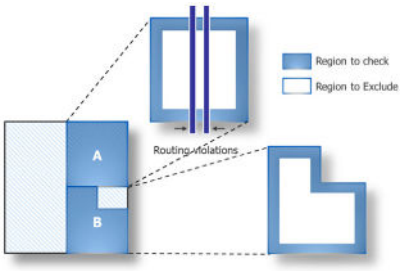
Using the Calibre nmDRC-Recon technology, a block designer can run targeted DRC verification on an incomplete block. If the Calibre nmDRC-Recon results are clean, the incomplete block can be passed to the chip designer, while the block designer runs the remaining rules in parallel on that block, speeding up the overall verification cycle.

Gray box exclusion

The Calibre nmDRC-Recon gray box feature allows designers to check top-level routing while ignoring cell details. The gray box designation removes data from a specified cell without removing geometries from the parent, allowing any routing violation over the specified cells to be captured. Designers can use a halo around removed geometries to capture interface violations between specified cells and their neighbors. Gray box exclusion also separates integration and routing violations associated with assembly from any immature block violations to enable designers to focus on interface and routing violations.

Gray box exclusion can be used for both rectangular and non-rectangular cells, although designers may need to specify the layer that represents the extent of non-rectangular cells (boundary layers can be used for this purpose).

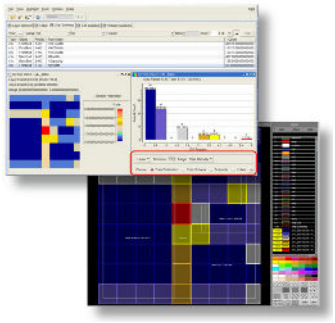
While removing geometries may introduce new DRC violations, designers can use the Calibre Auto-Waivers™ tool to waive any errors created by the exclusions. This allows designers to focus on the original (valid) DRC interface violations. All waived violations are saved to a waiver results database files for later review, as needed.



Gray box exclusion enables designers to exclude certain portions of the layout from DRC, while still allowing them to check those areas for interface or routing violations.

DRC Analyze

The Calibre nmDRC-Recon DRC Analyze function helps designers quickly analyze designs and view the distribution of errors to identify opportunities for quick enhancement of layout quality. Designers can draw different histograms (based on hierarchical cells or windows) for chip analysis, and specify custom scaling ranges. Colormaps can also be drawn, either on standalone windows or mapped on the design, to enable designers to probe down to error details (per cell and per window), where the results are shown distributed across the design. All analysis is done using the foundry rules deck without modification.



The Calibre nmDRC-Recon DRC Analyze function enables fast, in-depth visualization and analysis during error review and debugging.

Results

In tests on real-world designs, the Calibre nmDRC-Recon technology reduced overall DRC runtime by up to 14x while still checking ~50% of the total DRC set, which resulted in a 30% reduction in the total number of reported violations (compared to full-chip DRC). The DRC subset was effective in identifying floorplan and sub-chip integration issues that were meaningful to the targeted implementation stage, facilitating faster analysis and debugging.

As part of a growing suite of early-stage design verification technologies, the Calibre nmDRC-Recon solution enables designers to quickly and easily find and resolve selected physical integration issues early in the design cycle, accelerating design closure, and ensuring they deliver high-quality designs on schedule.

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