

TRAINING CENTER

TRIAS TRAINING CENTER

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TRIAS MIKROELEKTRONIK

ABOUT US

Since 1989 TRIAS mikroelektronik GmbH offers innovative product solutions for Design Automation (EDA) in the areas of FPGA and IC Design | Verification, as well as for ECAD in the form of a model-based E/E System Development platform for the development, manufacturing and service of wire harnesses and wiring systems.

Continuing education is an important topic and so we train our customers in innovative design and verification processes as well as in the use of our EDA and ECAD solutions.

Experienced TRIAS engineers support our customers with technical support, in consulting and in various services around our solutions.

Through intensive and competent consulting, customized solutions, and advanced trainings, we ensure Digitalization in Product Development - for shorter development times, improved quality, and increased reliability.

WE SUPPORT YOU IN YOUR DIGITAL TRANSFORMATION.

Note

Click on the spot ● in the header on the following pages for more information.



TRIAS TRAINING CENTER

TRIAS TRAININGS

Training is an important topic and so we train our customers in innovative design and verification processes as well as in the use of our EDA and ECAD solutions. Our Training Center educates our customers on FPGA design and verification, high-level languages (HDL) and signal integrity and also offers tool training. Thus, we make an important contribution to digitalization in product development.

- ▶ SystemVerilog – “Advanced Verification” for FPGA Design
- ▶ VHDL 2008
- ▶ Verilog for VHDL Users
- ▶ UVM Made Easy for FPGA Designer

- ▶ Accelerating FPGA and Digital ASIC Design
- ▶ Accelerating FPGA VHDL Verification and introducing UVVM

- ▶ Signal Integrity in PCB Design
- ▶ Design and validation of DDR interfaces on PCBs

- ▶ Tool Trainings for tools by Siemens EDA – formerly Mentor Graphic and Siemens Digital Industries Software



TRIAS TRAININGS

SYSTEMVERILOG – “ADVANCED VERIFICATION” FOR FPGA DESIGN ●

This workshop will provide an overview about the language SystemVerilog and introduce the new verification methodologies „Assertion Based Verification“, „Constrained Random Generation“ and „Functional Coverage“. Participants will learn how to use these powerful tools to speed up verification as well as to measure the verification progress and how these methodologies can be naturally applied to the verification of VHDL designs.

VHDL 2008 ●

The VHDL 2008 training course provides an overview about the changes and enhancements added to the language by the standard IEEE 1076-2008. The training is structured in three main areas, that cover new and changed synthesizable constructs, verification constructs that have been added coming from PSL (IEEE 1850). And in the final section the course will give an overview about how constrained randomization and functional coverage, which are not natively supported by the language, can be used with the OSVVM library.

VERILOG FOR VHDL USER ●

As designs become more complex and development times shrink, development teams increasingly need to leverage IP cores. This means that engineers must become "language-neutral" when dealing with HDL languages. They need a solid knowledge of VHDL and Verilog and the related design techniques.

Our workshop, with its fast and effective method, is suitable for experienced VHDL users to understand the differences, but also the similarities between VHDL and Verilog, and to master the Verilog-specific issues that could otherwise lead to difficult-to-identify problems.

We offer public, live online and on-site training.

For more information, visit our website at

[Training](#)

So they are always up to date.



TRIAS SCHULUNGEN

UVM MADE EASY FOR FPGA DESIGNER ●

Since the UVM library is very complex, building a testbench from scratch is a time-consuming task and requires a good knowledge of the tools the library provides. In order to help verification engineers to very quickly build a testbench the UVM Framework infrastructure has been developed. With UVM Framework it is possible to very rapidly create a UVM testbench and with a few changes the testbench is ready for simulation within a few hours.

The participants will create a UVM testbench in multiple steps using the UVM Framework. After the Workshop participants are able to use the UVM Framework API to create a testbench infrastructure for their own FPGA design.

ACCELERATING FPGA AND DIGITAL ASIC DESIGN ●

Implementing an FPGA or ASIC design does not just depend on knowing an HDL language. In addition to the knowledge of all language constructs, it is also important to structure the implementation in a suitable manner and to know advantages and disadvantages of different descriptions of the same behavior. If such approaches are consistently used, it will avoid many problems, which take a lot of time for causes to be found and solved, and thus reach their destination faster. The course will show how the development can be optimized and accelerated and also the quality of the design be improved.

▶ *Course in English language*

We also offer training as a live|online course - starting with one participant.

For more information, visit our website at

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TRIAS TRAINING

ACCELERATING FPGA VHDL VERIFICATION AND INTRODUCING UVVM ●

A significant part of the time for any FPGA project is taken up by verification. Reducing this time will accelerate the entire project development. The key to this is a well-structured testbench. This course focuses on FPGA verification and teaches how to build a testbench in a structured way. Theory alternates with practical examples and hands-on tutorials. It also covers important topics such as coverage, BFM, debugging and randomization. This course contains a general introduction to modern verification methodology and to UVVM (Universal VHDL Verification Methodology) – the world-wide #1 VHDL-FPGA verification methodology, and also the fastest growing verification methodology independent of HDL.

- ▶ *Course in English language*
- ▶ *Knowledge of VHDL prerequisite.*

SIGNAL INTEGRITY IN PCB DESIGN ●

This workshop is aimed at developers, who want to develop high-speed interfaces between semiconductor components, and complex board-level high-speed circuits. The training is suitable for developers, who not only design schematics, but also systems and layout. They will learn to judge when signal integrity becomes important, and relevant, e.g. to select the appropriate termination procedure. Signal reflection, and crosstalk effects are described, and demonstrated by simulation. Simulation examples are also demonstrated for common memory interfaces. You will learn how to implement high-speed bus systems, including clock design, load, and signal termination. In addition, the power distribution, and short circuits in the design are important issues.

- ▶ *As an optional training module the topics signal integrity issues and solutions for high-speed memory interfaces, and serial transceiver links can be offered.*

All courses are constantly revised.

For more information, visit our website at

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TRIAS TRAINING

DESIGN AND VALIDATION OF DDR INTERFACES ON PCBs ●

This workshop is for developers who want to implement high-speed memory interfaces on custom boards. Memory interfaces are very often used, they are faster and faster - and design problems are becoming more and more challenging. The training is suitable for developers who design not only schematics, but also systems and layout. You will become familiar with the peculiarities of memory modules for logical and physical designs.

Time and voltage tolerances are discussed. You will learn how to use signal integrity simulation to optimize the high-speed memory interfaces. IBIS models and simulation will reveal the effects and possible problem areas. You will learn how to implement high-speed memory slots, including on-board topics. In addition, the power supply problems are discussed. Finally, you will get to know board-level verification options.

TOOL TRAININGS FOR TOOLS BY SIEMENS EDA – FORMERLY MENTOR GRAPHICS AND SIEMENS DIGITAL INDUSTRIES SOFTWARE

We are pleased to offer a range of tool trainings that can also be tailored to your individual needs, including

- ▶ ModelSim/Quarta Core: HDL-Simulation
- ▶ ModelSim/Quarta Core: Advanced Topics
- ▶ Quarta Clock Domain Crossing Verification
- ▶ Quarta Formal Verification
- ▶ Capital Logic
- ▶ Capital HarnessXC
- ▶ Capital Wiring Designer Essentials
- ▶ Capital Harness Designer Essentials

This is only a small part of the list of available trainings, we are happy to inform and advise you on our entire offer.

All courses are constantly revised.

For more information, visit our website at

[Training](#)

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Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikroelektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products. TRIAS mikroelektronik is an Expert Partner of Siemens Digital Industries Software.

Siemens Digital Industries Software awards the status "Expert" to sales partners who have in depth expert knowledge in a product area or industry and have proven this repeatedly in reference projects

Hans Jürgen Schwender is certified by Siemens for the products Capital™| Capital™Essentials (formerly VeSys®) for the Automotive and Aerospace (Aero) markets and continuously undergoes a mandatory certification program to verify and expand his competencies.

COURSES

- ▶ **SystemVerilog – Advanced Verification for FPGA Design**
- ▶ **VHDL 2008**
- ▶ **Verilog for VHDL Users**
- ▶ **UVM Made Easy for FPGA Designer**
- ▶ **Tool trainings for tools by Siemens EDA**
- ▶ **Trainings for Capital™ and Capital™ Essentials**



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Dr.-Ing. Jürgen Wolde

studied theoretical electrical engineering and graduated with a degree in engineering. He then completed his doctorate in the field of electromagnetic compatibility to become a Doctor of Engineering. This followed the transition into the industry where he worked until 2005 in communications engineering at Alcatel. The scope ranged from ASIC design for products, to assembly designs and complex research designs using FPGA-based boards. Collaboration on a variety of studies and research projects, and management activities rounded off the range of applications.

He has been self employed since 2006, and has become a long-time partner of PLC2, TRIAS and other companies, where he works as a technical trainer worldwide. Jürgen Wolde is also the co-author of numerous presentations and scientific publications as well as co-owner of several patents.

COURSES

- ▶ **Signal Integrity in PCB Design**
- ▶ **Design and validation of DDR Interfaces on PCBs**



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Espen Tallaksen

is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement.

One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He is giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

COURSES

- ▶ **Accelerating FPGA and Digital ASIC Design**
- ▶ **Accelerating FPGA VHDL Verification**



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