

MODELSIM/QUESTA CORE: HDL SIMULATION

DESCRIPTION

ModelSim /Questa Core: HDL Simulation teaches users new to using ModelSim or Questa SIM for HDL simulation how to effectively use ModelSim/Questa Core to verify VHDL, Verilog, SystemVerilog, and mixed HDL designs.

You will learn how ModelSim/Questa Core supports HDL behavioral simulations, and some basic concepts in the digital design flow. Also, you will receive an introduction on how to invoke the Visualizer debug environment to debug the simulation results from Questa. Hands-on lab exercises will reinforce lecture and discussion topics and provide you with extensive tool usage experience under the guidance of our industry expert instructors.

AGENDA

- ▶ Invoke the ModelSim/Questa Core program
- ▶ Prepare VHDL and Verilog data for use by ModelSim/Questa Core
- ▶ Create and use design libraries
- ▶ Use ModelSim/Questa Core commands to run a simulation
- ▶ Invoke Visualizer Debug Environment
- ▶ Create a simple simulation script
- ▶ Use ModelSim/Questa Core for batch simulations
- ▶ Use the ModelSim/Questa Core Graphical User Interface
- ▶ Create a ModelSim/Questa Core project
- ▶ Simulate VHDL or Verilog designs
- ▶ Simulate mixed VHDL/Verilog designs

PREREQUISITES

- ▶ Some VHDL or Verilog knowledge
- ▶ Some familiarity with digital design concepts

DURATION

1 Day

LANGUAGE

English or German

COSTS

Upon request*

www.trias-mikro.com

**including training materials*



TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikroelektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.


We reserve the right to use another qualified trainer.


ADDITIONAL COURSE


▶ **ModelSim/ Questa Core: Advanced Topics**

Subject to change

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