VHDL-2008

DESCRIPTION

The VHDL 2008 training course provides an overview about the changes and enhancements added to the language by the standard IEEE 1076-2008. The training is structured in three main areas, that cover new and changed synthesizable constructs, verification constructs that have been added coming from PSL (IEEE 1850). And in the final section the course will give an overview about how constrained randomization and functional coverage, which are not natively supported by the language, can be used with the OSVVM library.

The attendee will learn the new and improved constructs for RTL design. In addition the new Assertion-Based Verification (ABV) methodology, coming from the PSL (IEEE 1850) language, will be discussed in detail complemented with the constrained randomization and function coverage additions that OSVVM provides. In hands-on labs the attendee will have the opportunity to use the enhanced language constructs, create assertions that describe specific sequential signal pattern, which are to be monitored for occurrence and for correctness, and to write randomized stimulus, and data oriented coverage models that will track the data values sent to the DUT.

AGENDA

- New and enhanced Features
  - Enhanced Generics
  - Hierarchical referencing
  - etc.
- Functional Verification : ABV
  - Layers
  - Boolean Expressions;
  - Temporal Expressions
  - Directives
  - Vunits
- Open Source VHDL Verification Methodology (OSVVM)
  - Randomizing using RandomPkg
  - Functional Coverage Using CoveragePkg
  - etc.

TARGET GROUP

Engineers with VHLD knowledge or basic knowledge of digital hardware design

PREREQUISITES

Basic knowledge of digital hardware design and good knowledge of VHDL

DURATION

2 days

LANGUAGES

English or German

COURSE TARGETS

- Mastering the new design capabilities and applying them on design examples
- Understanding of new verification features and how to use them in the own environment

COSTS

€ 1.400,00 per participant*

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Including training materials

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TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikro-elektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.

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ADDITIONAL COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- UVM Made Easy for FPGA Designers

Subject to change