09|2023

TRIAS TRAINING CENTER

UVM TESTBENCH MADE EASY

DESCRIPTION

Due to the complexity of the UVM library, creating a testbench is a time-consuming task and requires extensive knowledge of the capabilities offered by the library. To support verification engineers in the initial creation of a testbench infrastructure, the UVM framework was developed to create a UVM testbench very quickly. This can be simulated immediately and is adapted to the use case by making changes in some places using application-specific code.

After a short introduction to some UVM classes and expressions, the workshop UVM TESTBENCH EASY quickly turns to the details of the UVM framework.
The course is aimed at verification engineers with no prior UVM knowledge who want to get started using UVM testbenches.
The goal of the course is to create a complete UVM testbench using the Siemens EDA UVM Framework (UVMF), which is then supplemented with application-specific code in a few places.

The most important UVM building blocks are introduced, providing the basics of how a UVM testbench works, the process of creating instances, and the communication between the UVM components and the DUT. Based on this, the UVM framework verification building blocks and the YAML API are introduced.

AGENDA

- Introduction
- UVM Basics
- UVM Framework
- UVMF Base Classes
- Introducing the UVMF API
- Practical Example: Creation of a UVM Testbench
- Conclusion

TARGET GROUP
FPGA design or verification engineers

PREREQUISITES
Knowledge of SystemVerilog and OOP concepts

DURATION
2 days

LANGUAGES
English or German

COURSE TARGETS
- Create a UVM testbench with the UVM Framework
- In multiple steps to a simple example DUT
- Guidance to the process to run a testcase
- Ability to use the UVM Framework API for testbench for own FPGA design

COSTS
€ 1.400,00 per participant*

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**Including training materials*

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TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikro-elektronik GmbH since 2002 and, as the technical manager, covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.

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ADDITIONAL COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- Verilog for VHDL User

Subject to change