

# UVM TESTBENCH MADE EASY

## DESCRIPTION

Due to the complexity of the UVM library, creating a testbench is a time-consuming task and requires extensive knowledge of the capabilities offered by the library. To support verification engineers in the initial creation of a testbench infrastructure, the UVM framework was developed to create a UVM testbench very quickly. This can be simulated immediately and is adapted to the use case by making changes in some places using application-specific code.

After a short introduction to some UVM classes and expressions, the workshop UVM TESTBENCH EASY quickly turns to the details of the UVM framework.
The course is aimed at verification engineers with no prior UVM knowledge who want to get started using UVM testbenches.
The goal of the course is to create a complete UVM testbench using the Siemens EDA UVM Framework (UVMF), which is then supplemented with application-specific code in a few places.

The most important UVM building blocks are introduced, providing the basics of how a UVM testbench works, the process of creating instances, and the communication between the UVM components and the DUT. Based on this, the UVM framework verification building blocks and the YAML API are introduced.

## AGENDA

- Introduction
- UVM Basics
- UVM Framework
- UVMF Base Classes
- Introducing the UVMF API
- Practical Example: Creation of a UVM Testbench
- Conclusion

## TARGET GROUP

FPGA design or verification engineers

## PREREQUISITES

Knowledge of SystemVerilog and OOP concepts

## DURATION

2 days

## LANGUAGES

English or German

## COURSE TARGETS

- Create a UVM testbench with the UVM Framework
- In multiple steps to a simple example DUT
- Guidance to the process to run a testcase
- Ability to use the UVM Framework API for testbench for own FPGA design

## COSTS

upon request

www.trias-mikro.com


## TRAINER

**Alexandru Vlad Velea**
has an Electronics, Telecommunications and Information Technology University degree followed by MBA postgraduate degree.

From 2005 on he has been covering mostly the following Siemens products:
- HDL design, simulation and synthesis
- Wiring and harness design

He has a bright knowledge as consultant/ advisor/ technical support/ tools trainer. He is Wiring Harness consultant/ advisor for the Mentor Graphics / Siemens tools since 2011 and Digital IC flow (design/ simulation/ synthesis) consultant/ advisor for the Mentor Graphics/ Siemens tools starting 2005.

TRIAS is an Expert Partner of Siemens Digital Industries Software. Siemens Digital Industries Software awards the status "Expert" to sales partners who have in-depth expert knowledge in a product area or industry and have proven this repeatedly in reference projects.

Alexandru Vlad Velea is certified by Siemens for the products Capital | Capital Essentials (formerly VeSys®) for the automotive and aerospace (Aero) markets and continuously undergoes a mandatory certification program to verify and expand his competencies.

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ADDITIONAL COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- Verilog for VHDL User

Subject to change